Injection Locked Oscillators with Current Reuse

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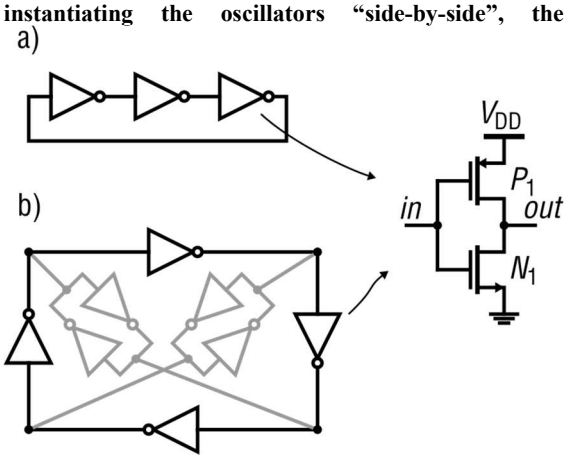
***Abstract*— Injection locking of oscillators is a known technique to improve the oscillator´s phase noise performance. Generally, this is done by running two or more oscillators that are linked through a passive or active coupling mechanism. Therefore, the power consumption (at least) doubles, leading to no improvement regarding the standard figure-of-merit (FoM). This work discloses a new coupling mechanism for locked oscillators, that reuses the supply current and builds upon the fact that inverters implemented in modern CMOS processes are able to reach reasonable oscillating frequencies even without using the full nominal supply voltage range. Instead of instantiating the oscillators "side-by-side", the proposed scheme stacks oscillators between the supply terminal, thus reusing the drawn current at the same time as dividing the available supply voltage among the oscillators. Aiming for proper voltage division, we exploit a property of the ring oscillators, in which they are able to keep the same power consumption while the number of phases is increased/decreased. In the presented approach, the phase-noise performance improves without a penalty in power consumption, thus also improving the FoM. Simulation results show that by coupling two oscillators at f_0 and $2f_0$, the higher frequency oscillator locks and inherits the better phase noise performance of the lower frequency oscillator, while reusing the same current, demonstrating the effectiveness of the proposed topology.**



Keywords—Oscillators, injection lock, coupling, current reuse

I. INTRODUCTION

Electrical oscillators are basic building blocks used in RF, analog, mixed-mode and digital circuits. Electrical oscillators can be generally categorized into linear and non-linear, being the linear based in a resonant mechanism and the non-linear based in a hysteresis mechanism. Coupling oscillators is used to ensure synchronization, improve phase-noise performance, or to allow the generation of quadrature signals or other multi-phase synchronous outputs [1,2]. Many types of coupling have been reported using direct injection locking [3-5] or specific feedback circuits as a phase-locked loop (PLL) structure [2,6,7]. Coupling to achieve quadrature outputs using active or passive coupling, have also been reported [8]. All these mechanisms have been reported with the underlying assumption that the oscillators are supplied by a V_{DD} voltage and that the source is also V_{DD}.

The basic ring oscillator has an odd number of inverters (Fig. 1 (a)), however many applications require quadrature signals or 4 or 8 phase signals. An even number of differential inverters can be used but then no longer simple CMOS inverters are used. Another approach is to add feedforward inverters [9-11], as represented in Fig. 1 (b).

The ring oscillators represented in Fig. 1 can be implemented with CMOS inverters and can both be studied as an RC oscillator being the R due to the transistors on-resistance and C as the node capacitance.

Fig. 1 (a) Basic odd-phase ring oscillator and (b) even-phase oscillator using feedforward inverters (gray inverters are weaker than the others).

For the oscillators in Fig. 1 a CMOS inverter is the basic cell, it has negligible static power (only due to leakage) and a dynamic power consumption (1):

$$P \propto C_l V_{DD}^2 \qquad (1)$$

where C_l is the output node capacitance and V_{DD} is simultaneously the power supply and output swing voltage (rail-to-rail), being the power proportional to the number of transitions per second.

In the past decades, the CMOS process trend has been to increase transistor speed at the same time as shrinking its size, consequently reducing the parasitic capacitances. To cope with the high-power density inherent to high levels of integration of active devices in a chip, the nominal operating voltage is reduced, together with the threshold voltage of the transistors. Under such circumstances, ring oscillators built with digital inverters can reach reasonable oscillating frequencies on the range of hundreds of megahertz even when using only half of the nominal supply voltage.

Thus, if only half of the nominal voltage is enough to provide a fundamental tone at a reasonable frequency, it is open the possibility of stacking multiple oscillators, and possibly reuse the current required to drive one of the oscillators to drive the next one on the cascade, instead of immediately feeding the current into the negative supply terminal [12].

Additionally, as the chip core operates with a low voltage in modern nodes (generally lower than 1 V for ultra-deep submicron processes), some sort of voltage step-down conversion is usually needed within the system, and this takes place very commonly on-chip. In such scenario, we could devise multiple stacked oscillators operating with the nominal supply voltage, at the price of having to cope with voltage limits of the technology, latch-up and other issues.

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Stacking different circuit blocks to reuse supply current comes with some challenges. Take the circuit from Fig. 2, that depicts two generic circuit blocks that are connected in series with a voltage supply V_{DD}. The circuits X_1 and X_2 can be modeled by load resistances R_{load1} and R_{load2}. The circuit X_1 is supplied with V_{DD}-V_x, while X_2 is supplied with V_x. With balanced loading, V_x is $V_{DD}/2$. If X_1 and X_2 are time-invariant from the V_{DD} perspective, V_x is constant. If, on the other hand, the loadings of X_1 and X_2 vary in time, as in oscillators, which tend to drain more power during transitions, V_x also varies and consequently also the fraction of V_{DD} allocated to each circuit. These interactions cause coupling between the circuits, and in the case of ring oscillators, they can cause injection lock.

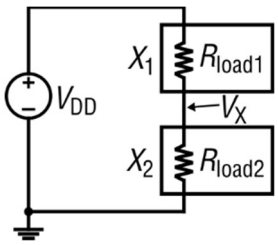

Fig. 2 Stacked loads.

In this paper, we propose a method to lock oscillators at integer multiple frequencies to improve phase noise performance without extra circuit elements and without a penalty in power consumption, taking advantage of the above-mentioned considerations. As it will be shown in Section II, the power consumption of ring oscillators using the same underlying inverters (even when working at different frequencies) have the same current consumption, allowing for current reuse. In Section III a comparative study using a commercially available 130nm CMOS technology show the feasibility and the advantages of the proposed technique. Finally, in Section IV, we draw conclusions and perspective future developments.

II. Underlying Circuit Assumptions

A. Ring Oscillator Power Consumption

The ring oscillators of Fig. 1 are implemented with standard cells inverters in a 130nm CMOS technology for several combinations of NMOS and PMOS. As an example, we show the power consumption results in Table 1 for one case of dimensioning (Library UMC Inv_Q (m=20), that corresponds to 20× W_P=600nm/W_N=530nm and $L_{N,P}$=120nm) having the others a similar behavior.

As can be observed from Table 1 for each circuit the power is almost equal while the frequency reduces by a factor of two each time the number of phases (loop inverters) doubles. The frequency effect is easily understood while the power consumption must be seen as "in each instant only a few inverters are changing" (Fig. 3), being all the others seated at a high or low voltage. While only the inverters changing state are consuming energy it becomes independent of the total number of inverters that only affects the total time for a period. Furthermore, it also happens that the total current drawn is approximately constant during the whole period, as represented in Fig. 4 for the case of 8-phase oscillator. It can also be seen, in Fig. 4, that the current carries spikes relative to the 8-phase (8-inverters ring) oscillator. This means that we can use oscillators at different frequencies implemented with equal inverters and reusing the same current, while the AC component of this current will cause the injection lock of the oscillators.

TABLE I. Odd and Even Phase Oscillator Power & Freq.

Ring Oscillator		Power [mW]	Frequency [MHz]
Fig.1(a) # phases	5	5.24	6 915
	9	5.26	3 948
	17	5.26	2 047
	33	5.26	1 057
	65	5.27	538
Fig.1(b) # phases	4	13.16	7 352
	8	13.50	3 533
	16	13.51	1 771
	32	13.51	887
	64	13.51	444

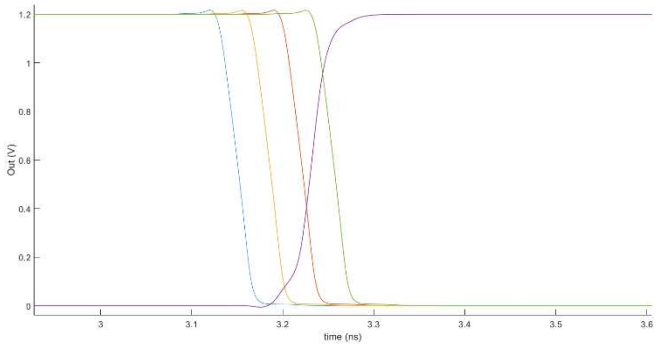

Fig. 3 Snapshot of selected inverters output during one period.

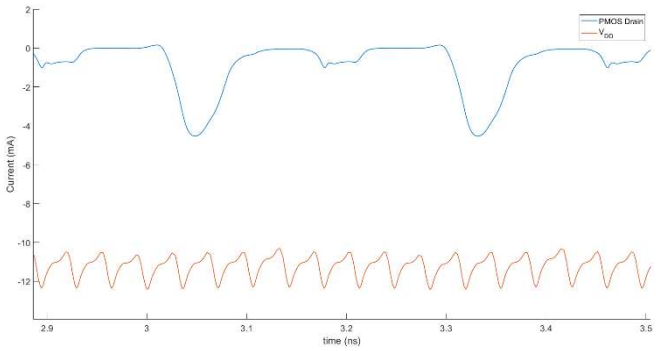

Fig. 4 Snapshot of current drawn from V_{DD}, from a single inverter and from an 8-phases oscillator.

B. Oscillators Injection Locking Mechanisms

In the case of PLL based locking mechanisms one of the objectives is, usually, to inherit the excellent phase noise performance of a mechanical element (crystal) to improve the phase noise performance of an electronic circuit. This is accomplished in within the bandwidth of the PLL.

When coupling similar types of oscillators, simpler mechanisms are used, either active or passive [8] with improvement in the phase noise performance [2, 8]. The commonly used strategy is shown in Fig. 5, where two equal

TABLE II. 32 AND 64 PHASE OSCILLATOR PERFORMANCE UNDER DIFFERENT COUPLING TOPOLOGIES.

	#-Phase	Power [mW]	Frequency [MHz]	PN [dBc/Hz] (@100kHz)	PN [dBc/Hz] (@1MHz)	PN [dBc/Hz] (@10MHz)	FoM (@10MHz)
Single V_{DD}=1.2V	32	13.5	887	-80.8	-109.9	-135.1	-162.8
	64	13.5	444	-89.7	-118.0	-141.7	-163.4
	128	13.5	222	-98.5	-125.7	-148.1	-163.7
Single V_{DD}=0.6V	32	0.8	**276**	-88.5	-114.3	**-135.7**	**-165.4**
	64	0.8	138	-96.8	-121.1	-141.8	-165.5
	128	0.8	69	-104.7	-127.5	-147.8	-165.4
Side-by-side V_{DD}=0.6V	32/64	1.6	**276**/138	-97.0	-121.7	**-142.6**	**-169.2**/-163.2
Side-by-side V_{DD}=0.6V	(2×) 64	1.6	138	-97.0	-121.7	-142.6	-163.2
Stack V_{DD}=1.2V	32	1.6	**276**	-92.6	-116.5	**-137.9**	**-163.9**
	64	1.6	138	-98.5	-123.1	-143.9	-164.9
Stack V_{DD}=1.2V	(2×) 64	1.6	138	-99.2	-123.4	-144.1	-164.9
Stack V_{DD}=1.2V	32	1.6	**276**	-92.9	-117.7	**-137.9**	**-165.4**
	128	1.6	69	-105.5	-129.5	-148.2	-162.8

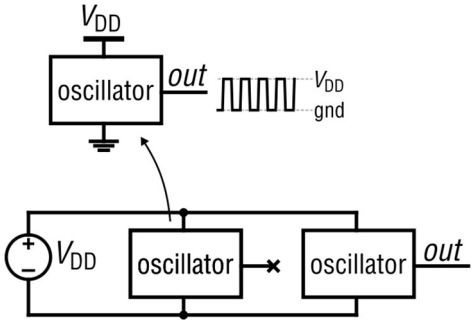

Fig. 5 Locking of oscillators in "side-by-side" (V_{DD} has an internal series resistance=1Ω).

oscillators are coupled resulting in a phase noise improvement of 3dB while the power also doubles resulting in a neutral balance in the conventional FoM (2) number.

$$\text{FoM} = \mathcal{L}_{\text{measured}} + 10\log\left(\left(\frac{\Delta f}{f}\right)^2 \frac{P_{DC}}{P_{ref}}\right) \quad (2)$$

The locking mechanism is most times explicit, implemented with dedicated components to ensure strong coupling (a differential pair, resistors or capacitors) but it can also be through circuit non-idealities or parasitics (substrate, common mode nodes with non-ideal zero/infinity resistance, etc.).

Therefore we envisage that we can couple two oscillators by stacking them at different voltage planes, improving phase noise while reusing current. This improvement can also be leverage by locking oscillators at different (multiple) frequencies making the faster oscillator inheriting the better phase noise performance of the slower oscillator. The proposed topology is presented in the next section.

III. PROPOSED TOPOLOGY

The proposed and studied topology is shown in Fig. 6. The floating node between oscillators will allow for the in-phase coupling mechanism of two even-phase oscillators. For clarity we show an example where we have a V_{DD} of 1.2V, with similar oscillators, with 32, 64 and 128 phases, each operating 0.6V at different planes, reusing the same current and being locked in phase and frequency.

Due to the long convergence and simulation times required to simulate the oscillators the comparison study is restricted to the case of 32, 64 and 128 phases oscillators and the combinations among them. The results for the circuits represented in Fig. 7 are shown in Table II.

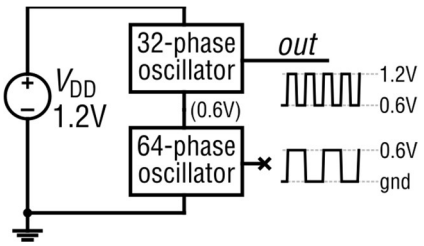

Fig. 6 Locking of oscillators in "stack" (example with 32 and 64 phases).

Several interesting results can be observed from Table II:

1) Single oscillators exhibit, as expected, a phase noise performance improvement over 6dB at the same frequency offset due to the increase in the number of inverters in the loop and to the larger relative distance to the center frequency; The much higher power consumption is due to the higher operating voltage, much higher than the transistors' threshold voltage and the higher operating frequency.

2) side-by-side oscillators show marginal improvement due to very weak coupling (it is being carried out by the voltage supply non-ideal series resistance with a 1Ω value); it would

be required an explicit coupling mechanism to further improve the phase-noise.

3) Stack oscillators, have better phase noise performance than single or side-by-side oscillators;

4) the higher frequency oscillator on the stack structure inherits the good phase noise performance of the slower one and the difference is marginal when compared with two stacked slower oscillators;

5) Benefiting from current reuse the stacked oscillators can lead to significant improvements in the FoM of the faster clocks.

6) In the context where the oscillators are operating with supply voltage lower than the LDO voltage the difference would further benefit the stack structure.

7) In the context where it is required a divider the proposed approach allows for a "free" divider for ratios of powers of 2

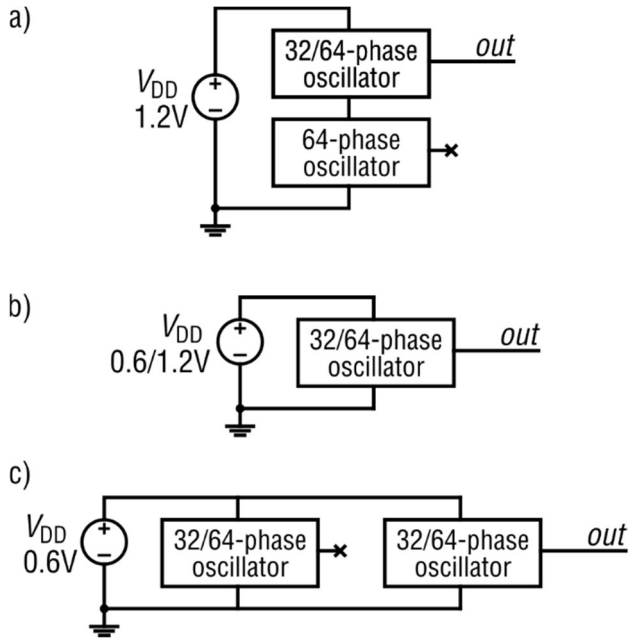

Fig. 7 Topologies tested and Simulated leading to the results shown in Table II (illustrated for 32 and 64 phases) .

IV. Conclusions

In this paper it is shown that ring oscillators designed with the same native inverter lead to a defined drive current that does not depend in first order with the number of inverters, only the frequency changes. With the above result in mind it is proposed to couple oscillators in a stack structure to allow current reuse. By doing so either we have two oscillators working at $V_{DD}/2$ or even more advantageous if V_{DD} is obtained from a higher shared supply voltage by an LDO, as it commonly exists in many circuits. In this case it would further improve efficiency and therefore the FoM. Locking at multiple frequencies with a stack topology can be an interesting way to obtain improved phase-noise performance at higher frequencies without a penalty in power consumption, or, when operated by batteries, in the total charge drawn from the battery.

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