A Small-Footprint Quasi-Passive 1st Order ΣΔ Modulator

Gonçalo Rodrigues, Jorge Fernandes, Taimur Rabuske
INESC-ID Lisboa, Instituto Superior Técnico, Universidade de Lisboa, Portugal
{goncalo.rodrigues, jorge.fernandes, taimur.rabuske}@inesc-id.pt

***Abstract*— Discrete-time ΣΔ generally rely on switched-capacitor implementations that require operational amplifiers to implement the integrators. For ultra-deep submicron processes, the limited intrinsic gain of the transistor hinders the design of operational amplifiers. This paper proposes a topology for ΣΔ modulators that employs a low-power quasi-passive integrator. The input voltage is converted into the charge-domain by a transconductor-based front-end. The integration process is implemented with MOS capacitors instead of linear capacitors, which allows the reduction of charge leakage. While this design targets relatively low resolutions, due to the nonlinear nature of the passive integration, the absence of operational amplifiers enables the topology to fit in a very small area. The topology is validated by simulations with the design of a 1st order ΣΔ modulator. The circuit is designed in a 0.13 µm technology, fits in 40 x 60 µm², performs at 100 MSps with 51.34 dB of SNDR and consumes 0.08 mW.**

Keywords— ΣΔ ADC, Passive Integration, Low-power, IoT, Small Circuit

I. Introduction

Although most of the information that we perceive in the world is analog, transmission and processing of information in electronic systems are increasingly done in the digital domain. Consequently, the demand for Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) has increased due to the need of bridging these domains [1]-[3]. If energy is limited, such as in a battery-powered device, these ADCs and DACs must present low-power consumptions.

ΣΔ ADCs employing oversampling and noise shaping techniques have been widely used for different applications due to their ability to trade-off bandwidth and accuracy. ΣΔ modulators can be broadly categorized into discrete time (DT) and continuous time (CT) [4]. Nevertheless, typical implementations of both classes of ΣΔ modulator require active integrators. These integrators generally demand operational amplifiers with high unity-gain frequency requirements, which are increasingly difficult to be achieved in short channel CMOS technologies due to the limited intrinsic gain of the transistors. Alternatively, some works were recently proposed with passive SC integrators [5]-[8] resulting in low power and high-speed modulators.

These implementations are not affected by short channel lengths, which represents an advantage over the active counterparts. The biggest drawback, however, is the fact that passive integrators are lossy, causing distortion on the ADC output. The authors in [7] propose a SC-integrator implemented with MOS capacitors (MOSCAPs), taking advantage of the variable capacitance of MOSCAP to reduce charge leakage during integration. The passive integration was demonstrated within a second order single stage ΣΔ modulator and in a MASH 2-2 modulator [8], replacing one of the active integrators by a passive implementation.

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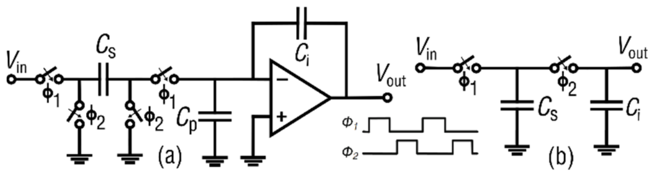

Fig. 1. (a) Active SC integrator (b) Passive SC integrator

In this paper we present a quasi-passive 1st order ΣΔ ADC employing a transconductor to transform the input voltage into current. The resulting current is then integrated into the charge-domain in the MOSCAPs. We demonstrate that with proper biasing of the MOSCAPs, the negative feedback loop that is inherent to the ΣΔ modulator ensures that the integration takes place at the zone of minimum charge loss.

The topology is demonstrated by the implementation of a ΣΔ modulator prototype in a 0.13 um process. Simulation results show that the ADC consumes 0.08 mW while sampling at 100 MSps. For an OSR of 128, the circuit performs with an SNDR of 51.34 dB, leading to an ENOB of 8.23 bits. The resolution is limited by the nonlinear property of the passive integration, that is leaky because of the MOSCAP parasitic capacitances. Due to the absence of high-gain amplifiers, the circuit can fit in a very small area of approximately 40 x 60 µm².

The remaining of this paper is organized as follows: in Section II, we describe the working principle of the ΣΔ ADC together with an introduction to the charge-mode front-end. Section III presents the circuit level implementation and transfer function. The results of the charge mode and the whole ADC are presented in Section IV. And finally, Section V presents the main conclusions.

II. Operation Principle

A typical switched-capacitor integrator, containing an opamp, is shown in Fig. 1a. The dynamic properties of the opamp, such as the unity-gain frequency and slew rate determine the speed of the integration, while the dc voltage gain establishes the quality of the integration function. Thus, a SC integrator realized with an opamp with finite gain exhibits integration leakage and is therefore lossy. Lossy integrators weaken the noise-shaping ability of the modulator, leading to a degraded signal-to-noise-and-distortion ratio (SNDR) [9]. The transfer function of the circuit shown in Fig. 1a is given by:

$$\frac{v_{out}}{v_{in}} = \frac{\alpha z^{-1}}{1 - \beta z^{-1}} \tag{1}$$

With infinite gain on the opamp, α is given by C_S/C_i and β = 1. With finite gain, β is then given by:

$$\beta = \frac{A_0 C_i + C_i + C_p}{A_0 C_i + C_i + C_p + C_S} \tag{2}$$

Where A_0 is the open-loop gain of the opamp. In practice, as the value of A_0 decreases, the value of β further deviates from

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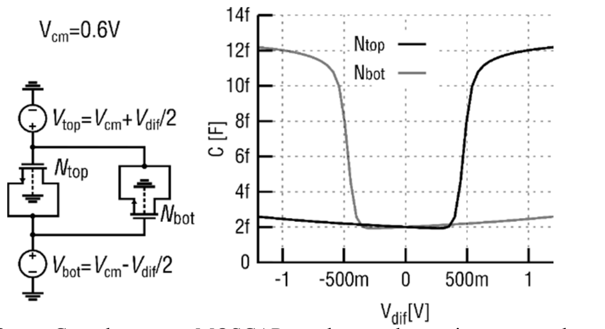

Fig. 2. Complementary MOSCAP topology and capacitance vs. voltage behavior of the MOSCAPS.

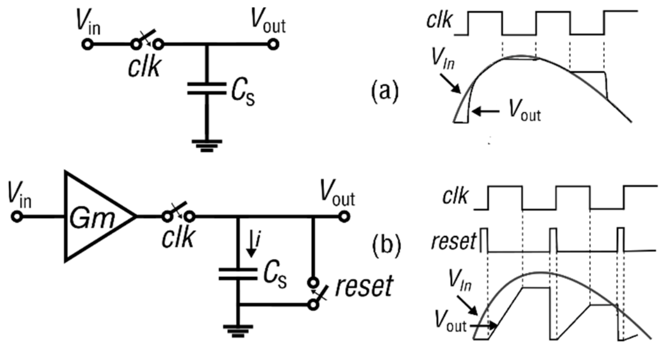

Fig. 3. (a) Track and Hold (T/H) (b) Integrator and Hold (I/H)

the ideal unity, and the integrator becomes leakier and performs worse in terms of SNDR.

A. Passive Integration

To avoid power hungry amplifiers and its design difficulties, a passive SC integrator can be used. The main idea of the circuit is depicted in Fig. 1b. Similarly to the active implementation, the circuit is controlled by two non-overlapping clocks ϕ_1 and ϕ_2. The input signal is sampled in capacitor C_s during ϕ_1 and then the charge is transferred to C_i during ϕ_2. Finally, before the next integration takes place, C_s is disconnected from C_i. While the voltage on C_i is not affected by disconnecting C_s (assuming ideal switches), the integration takes place on the charge domain, and some charge is still "leaked" given the fact that C_s has a non-zero value of capacitance. This affects the modulator performance in a similar way to leakage caused by finite amplifier gain in an active ΣΔ modulator. For the passive case, α and β are given by:

$$\alpha = \frac{C_s}{C_i + C_s}, \beta = \frac{C_i}{C_i + C_s} \tag{3}$$

Notice that β in (1) and (2) are identical if we use $A_0 = 0$, which is reasonable since we are using no amplifier at all. The absence of A_0 as a knob in β makes the design of high-accuracy passive SD modulators much more challenging. While the integrator leakage can be calibrated digitally [9], in this work we focus in evaluating the potential of passive integrator implementations without any sort of error correction.

In order to reduce the leakage on the passive-integrator, we must reduce the proportion of total charge that is lost while disconnecting C_s from C_i (and thus the relationship C_s/C_i at that instant). At the same time, C_s cannot be made too small in a SD implementation, because the integrator dynamic range is also function of C_s/C_i. A solution to these issues is to use a capacitor with variable capacitance: C_s should be relatively large while sampling, and present the minimum possible capacitance during integration, so that the leaked charge is minimized.

In the context of an integrated circuit, a MOSCAP is a good candidate for such device, and its properties have been already explored towards amplification, with the "parametric amplifier" [10,11]. The parametric amplifier is, in essence, a track-and-hold that samples with high-capacitance and "holds" with low-capacitance, which is the same principle that we are targeting.

In [7,8] the authors achieve this principle by changing dynamically the body bias voltage of the MOSCAPs. In this work, on the other hand, we will explore a circuit that is similar to the one proposed in [12] to achieve the same purpose without dynamic body biasing. The concept is demonstrated in Fig. 2 where the capacitance vs. voltage behavior of the MOSCAPS is shown for a complementary MOSCAP topology. The main idea is to bias the MOSCAPs outside the low capacitance zone while sampling, and guarantee that the charge processing (integration) takes place inside this zone. Luckily, the negative feedback loop that is inherent to the ΣΔ modulator greatly helps in this task. The principle will be further explained in Section III.

B. Integrator and Hold

Traditional ADCs use a Track and Hold (T/H) circuit on the input, which allows to track the input voltage and hold its value to be quantized, Fig. 3a. The T/H is a voltage-based circuit, and consequently cannot be used with MOSCAPs that present a variable capacitance if we do the processing in the charge domain.

In [13], the authors present a transconductance-based sampling circuit that operates on the charge domain. It does so by first converting the input voltage into an output current. This current is then integrated as charge into the gate capacitance of a MOSCAP. Therefore, even though the MOSCAP presents a non-linear capacitance vs. voltage behavior, the integrated charge is a linear function of the integration time, transconductance and input voltage. Additionally, this Gm-based frontend presents a *sinc* filter response that helps to increase tolerance to clock jitter, time skew, non-zero rise and fall times of the sampling clock and switch resistance when compared to T/H as explained in [14] and [15].

Considering the Gm cell as a perfect transconductor with gain g_m, the charge that is transferred to the sampling MOSCAP is given by (4).

$$Q = V_{out} \times C_s \Leftrightarrow \int_0^{T_s} (V_{in} \times g_m)\, dt = V_{out} \times C_s \tag{4}$$

Where Ts is the integration time, V_{in} the input voltage, V_{out} the output voltage and C_s the capacitance of the sampling MOSCAP.

According to (4) the charge is linearly dependent of Ts, V_{in}, and g_m, thus to increase/decrease the amount of charge Q there are three variables that can changed.

C. Complete ΣΔ modulator

Fig. 4a. presents the top-level architecture of the passive ΣΔ modulator. For simplicity, all MOSCAPs are represented by symbols of linear capacitors. The corresponding circuit waveforms for 3 clock cycles are presented in Fig. 4b. The implemented modulator operates differentially.

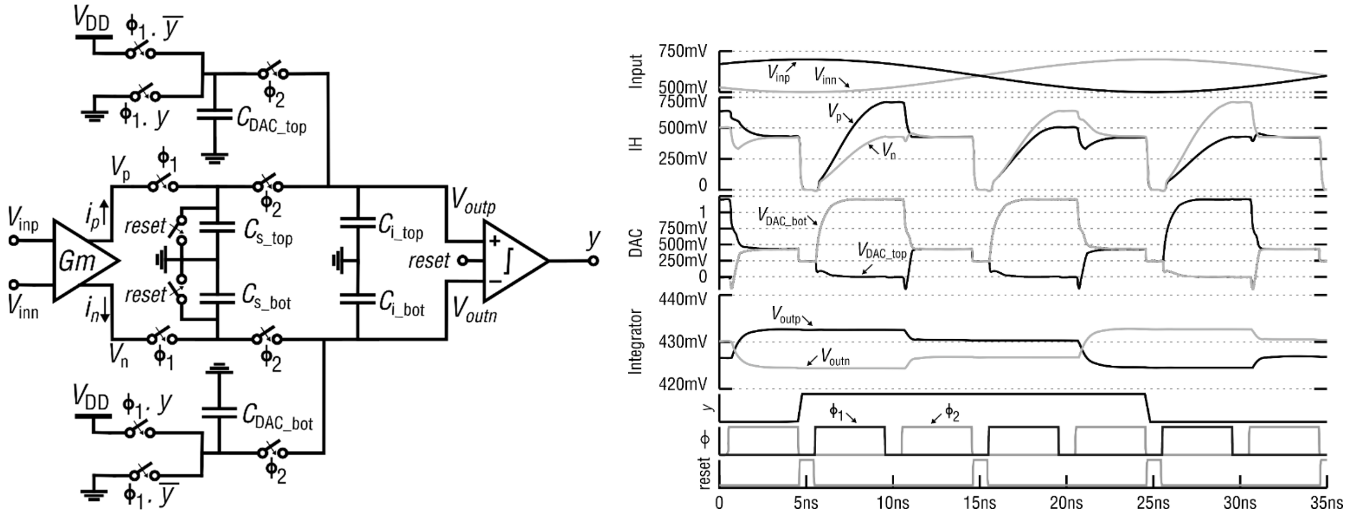

Fig. 4. (a) Top level schematic of the ΣΔ modulator (b) Simulation waveforms.

Initially, the input voltages are converted into linear currents i_p and i_n, with the Gm cell. The two currents are then transferred to the sampling MOSCAPs, C_{s_top} and C_{s_bot} respectively, a high linearity is needed in this conversion as it will affect the overall performance of the modulator.

Following the signal path, the charge that is stored in the sampling capacitors (C_{s_top} and C_{s_bot}) is transferred to the integrating capacitors (C_{i_top} and C_{i_bot}). The capacitance of C_{i_top} and C_{i_bot} are designed to be 10 times larger than C_{s_top} and C_{s_bot} to reduce the charge leakage. Once the charge transfer is complete, the voltages in C_{i_top} and C_{i_bot} are measured by a latched comparator. Based on the result, represented in Fig. 4b by y, a feedback is generated, switching the bottom plates of the DAC to the positive or negative reference (supply voltage or ground respectively) as shown by V_{DAC_top} and V_{DAC_bot}.

Also, during the sampling process of the input signal, the DAC capacitors are connected to V_{dd} or *gnd* according to the output of the comparator. The charge in C_{DAC} and C_s is transferred to C_i concurrently to C_s, and the voltages across the integrating capacitors are measured by the comparator to generate a new result.

Between each cycle, a reset signal is used to completely discharge the sampling capacitors and to activate the latched comparator. The resulting word from the comparator output, is a digital conversion of the analog input signal.

III. Implementation

A. Gm cell

The Gm cell is a crucial component of the integrator and hold as it converts the input voltage into a current with a variable gain. The circuit employed in this work is based on the design proposed in [13]. The Gm cell uses an inverting amplifier which is a circuit widely used in both analog and digital circuits. In digital circuits, the inverter implements the Boolean operation of negation or inversion. In analog circuits, the inverter is used to achieve amplification.

Fig. 5. shows the schematic of the implemented circuit which exploits the inverter transconductance mode and uses source degeneration, that is also used for common mode feedback (CMFB). This Gm cell is used to convert continuously the input voltage to an output current, with a variable gain that can be controlled by the number of cells that are used in parallel and by the width and length of the different transistors. In order to evaluate the linearity of the integrator and hold, and size the different components, a Verilog-A block was created to measure the charge that is transferred to the sampling MOSCAP during each clock period. The implemented code is based on a simple equation that relates the charge with current and time: $Q = I * t$, being implemented in a double ended block and measuring the current that flows to the MOSCAPs on the positive and negative end. The current is integrated in time in order to obtain the charge of each integration and the result is saved in a file in order to measure its linearity with ENOB, SNDR and THD.

For the I/H implementation, two helpful expressions ((5) and (6)) can be derived from (4) which express the differential and common mode voltage at the output of the Gm cell.

$$V_{CMout} = \frac{V_{outp} + V_{outn}}{2} = \frac{V_{CMin} \times g_m \times T_s}{C_s} \qquad (5)$$

$$V_{difout} = V_{outp} - V_{outn} = \frac{V_{difin} \times g_m \times T_s}{C_s} \qquad (6)$$

With equations (5) and (6) and testing different transistors size combinations by measuring the results with the implemented code, the transistors size of the final Gm cell is presented in table I. Both NMOS and PMOS transistors are implemented with a channel length of 500 nm for high output impedance and low 1/f noise [13].

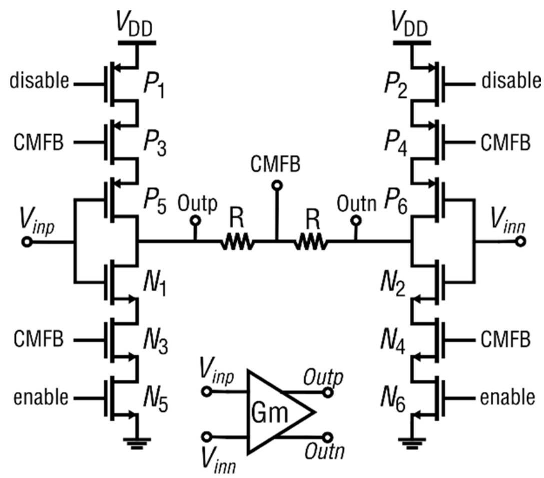

Fig. 5. Transistor level Gm cell.

TABLE I. I/H TRANSISTOR SIZE

Transistor	Width (µm)	Length (µm)
PM1 / PM2	2	0.5
PM3 / PM4	2	0.5
PM5 / PM6	5	0.5
NM1 / NM2	2	0.5
NM3 / NM4	0.5	0.5
NM5 / NM6	0.25	0.5

The sensing resistances are set to 50 KΩ to avoid excessive charge leakage and at the same time to allow the CMFB.

The Gm cell transconductance was estimated to be 23 µS presenting a charge linearity of 12.03 bits.

B. Sampling and DAC MOSCAPs

Sampling and DAC MOSCAPs are implemented with the same topology as the one previously shown in Fig. 2. This complementary topology allows to charge the MOSCAPs in the high capacitance region and to accommodate the double ended structure of the ADC.

MOSCAPs W size are set to minimum (160 nm) in order to achieve a low W/L ratio, which according to [12] enhance the difference of capacitance presented by the MOSCAP for the two working regions. To size the sampling MOSCAP four important aspects must be considered. The first one is the linearity of the charge transfer which must maximized. The second one is to have a high enough capacitance so that the MOSCAP does not saturate or start charging in voltage mode. The third is to achieve a common mode voltage at the output of the Gm cell greater than 0.5 V to bias the MOSCAPs at the maximum capacity. And finally, the output differential voltage must be large in order to achieve a wide dynamic range inside the ΣΔ modulator.

With this reasoning C_S was set to 300 fF, being implemented with 12 MOSCAPs in parallel (m = 12) with a length of 12 µm in order to accumulate the charge produced by the Gm cell and comply with the I/H requirements.

Considering that DAC MOSCAPs are connected to V_{dd} or *gnd*, its capacitance must be considerably smaller than C_s in order to avoid modulator saturation. C_{DAC} was therefore implemented with 160 nm of W and 4.3 µm of L and m = 2.

C. Latched comparator

The employed comparator is a StrongARM latch [16] that is optimized for low power following the procedure described in [17]. The comparator is designed to have an input-referred noise of approximately 0.1 mV. This comparator was reused from a previous design that had slightly more demanding specifications. Since the comparator is not custom-tailored for this SD modulator, the power efficiency of the current implementation has room for improvements.

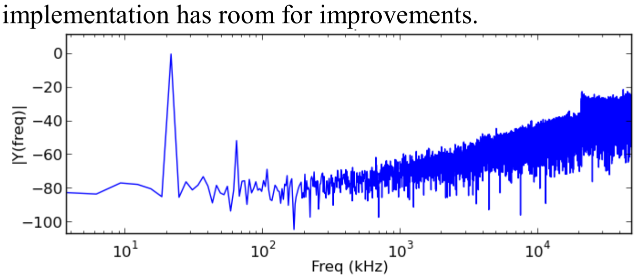

Fig. 6. ΣΔ Modulator FFT for a 21.36 kHz input signal.

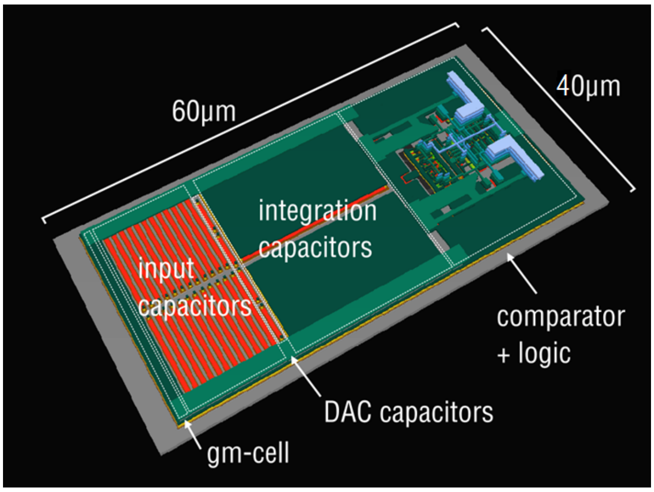

Fig. 7. ΣΔ Modulator circuit layout

IV. SIMULATION RESULTS.

For the charge front-end, which includes the Gm cell and the sampling capacitors, an ENOB of 12.03 bits was achieved for a 200 mV input at a frequency of approximately 24.414 kHz and with a sampling frequency of 100 MHz.

For the whole ΣΔ modulator, performing an analysis with 32768 points with an input frequency of approximately 21.36 kHz and an OSR of 128, an SNDR of 51.34 dB was achieved which translates in a 8.23 ENOB. The resulting FFT is presented in Fig. 6. The power consumption of the modulator was 0.08 mW having a supply voltage of 1.2V and presenting a small area of 40 x 60 µm^2 as shown in Fig. 7.

V. CONCLUSION

With this work we implemented a 1st order ΣΔ modulator without amplifiers to perform the integration process. A small size, low power circuit was achieved which are two valuable aspects for battery-powered portable devices. The area and the power consumption can be further decreased without affecting the performance, as the comparator was over dimensioned for the modulator performance.

For the implemented circuit, the 1st ΣΔ modulator achieves an ENOB of 8.23 bits, targeting relatively low resolution applications. Nevertheless, the circuit presents a very small area of 40 x 60 µm^2 and a power consumption of 0.08 mW which can be further decreased in future implementations.

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