A sub-μW 3–10MHz Stacked Oscillator with a Duty-Cycle Calibrated Level Shifter

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***Abstract*—The ring oscillator is the topology of choice in many modern applications given its simplicity, small area footprint, low-power and ability of being implemented with digital inverters. The oscillation frequency is dictated by the number of stages in the chain and the average delay of the inverters. In deep submicron processes, the very short propagation delay of logic gates makes the ring oscillator a very energy-efficient solution for high frequencies of operation, whereas for low frequencies the efficiency generally drops because larger capacitances must be driven to slow down the transitions. In this paper we propose a topology of oscillator that employs four injection-locked stacked ring oscillators, reusing current while the available supply potential is divided among these stages, naturally reducing the oscillation frequency while maintaining energy efficiency. The output signal is recovered to the supply rails through a level shifter circuit with feedback, allowing to adjust its threshold to deal with PVT variations. Simulation results show that the circuit operates from 3–10 MHz, while consuming 0.7 μW at 10 MHz, with a phase noise of -88.8 dBc/Hz at 100 kHz offset, leading to a FoM of -160 dB.**

***Index Terms*—Ring oscillator, stacked oscillator, duty-cycle calibration, current-starved inverter.**

I. Introduction

Short-range IoT applications are usually supplied by a battery or a power harvesting circuit resulting in the demand for extremely low-power consumption circuit solutions. Furthermore, to enable extensive deployment, full integration and small-die area (lower-cost) are common goals.

An IoT node has RF, analog, mixed-mode and digital blocks, all raising the demand for an oscillator circuit of some sort. The simplicity, feasibility under low voltage power supplies and possibility to fit in a small die area favor the choice of ring oscillators instead of relaxation or LC oscillators. Conventional ring oscillators use an odd number (n) of CMOS inverters, having the oscillation frequency given by

$$f_1 = \frac{1}{2 \cdot n \cdot t_d}, \tag{1}$$

while the dynamic power consumption is given by

$$P = f_1 \cdot C_1 \cdot V_{DD}^2, \tag{2}$$

where t_d is the inverter delay, C_1 is the total switching capacitance and V_{DD} is simultaneously the power supply and output swing voltage (rail-to-rail) [1]. To design a ring oscillator in deep submicron technology nodes, where the inverters have a very short delay, may be extremely power inefficient when the target frequency is relatively low, in the MHz range. The common approaches to reduce the oscillation frequency (by increasing t_d) tipically include employing: (a) a large number of inverters; (b) additional capacitors in the intermediate nodes; (c) transistors with enlarged length (L) leading simultaneously to an increase in transistor capacitance and triode resistance; (d) starved inverters. While (a-c) simultaneously increase die area and power, (d) see the "starving" transistors of the current sources leaving saturation and distorting the output curves.

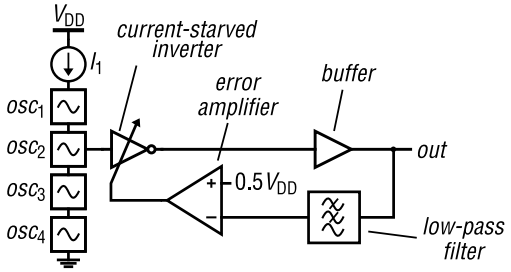

Fig. 1. Block diagram of the proposed low-power oscillator circuit.

On the other hand, an inverter delay can also be increased if we reduce the power supply voltage (V_{DD}), which also reduces the circuit power consumption, especially if the transistors are operating in the sub-threshold region. However, the use of a low V_{DD} oscillator requires an LDO circuit, or some sort of voltage limiting circuit, reducing the energy efficiency gains. In [2] it is shown that the use of 2 stacked oscillators produce a virtual intermediate node voltage (similar to the reduction of the oscillator supply voltage to $V_{DD}/2$), reusing the same current, and locking both oscillators in frequency.

In this paper we further explore the reduction of power supply towards sub-threshold operation of the inverters by stacking 4 ring oscillators under a regular supply voltage of 0.9 V, benefiting simultaneously the power consumption (current reduction and current reuse) and the phase noise (PN) improved by injection lock. In Section II we propose the complete circuit: a current controlled oscillator (ICO) with 4 stacked oscillators with a level shifter for rail-to-rail output, and a low-power consumption feedback loop to calibrate the frequency duty-cycle and ensure that the circuit is robust to process and mismatches (see Fig. 1). In Sections III and IV we show in detail the circuit blocks using a commercially available 130 nm CMOS technology and, in Section V, we present and discuss the results showing the feasibility and the advantages of the proposed techniques. Finally, in Section VI, we discuss the results and draw conclusions.

II. Proposed Architecture

In this work we propose a ring oscillator with improved PN and a low-power level shifter that uses an active background duty-cycle calibration feedback loop, as shown in Fig. 1. The

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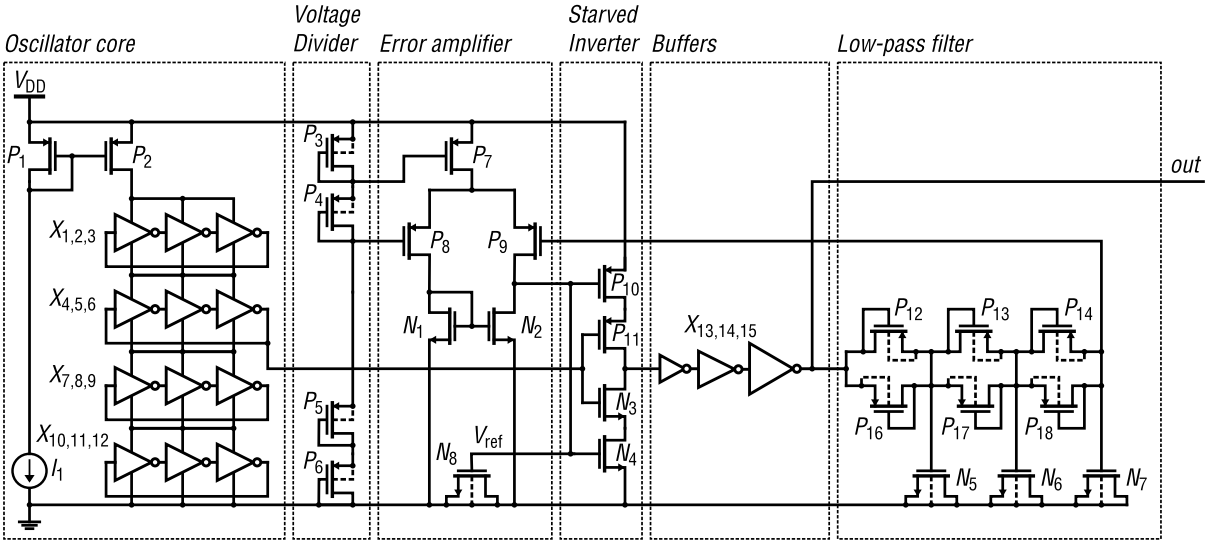

Fig. 2. Complete schematic of the proposed current-controlled oscillator with feedback loop to control the threshold of the level shifter.

PN is improved by current-reuse based injection lock, and the level shifter assures a 50% duty-cycle rail-to-rail signal.

The full schematic of the proposed current-controller oscillator is presented in Fig. 2, and comprises the stacked ring oscillator core, a voltage divider (used as reference for the feedback loop) and a level shifter composed by an error amplifier (EA), a current-starved inverter with reconfigurable threshold, digital buffers and an all-MOS low-pass filter with low-cutoff frequency made with MOS pseudo-resistors and MOSCAPs. The circuit blocks are explained in the following sections.

III. Oscillator Core

The oscillator core is composed by four stacked ring oscillators, each one comprising three single-ended conventional digital inverters. The frequency is tuned by a bias current which limits the switching speed of all the inverters simultaneously.

In the context of low-frequency oscillators, there are two main advantages on implementing the oscillator core with a stack of ring oscillators: the frequency is lowered at no power penalty due to increased load capacitance; the PN is improved due to the current-based injection lock mechanism. In Fig. 4 we see that the supply voltage is divided equally among the ring oscillators, resulting in four output waves with ~215 mV_{pp}, while the periods are exactly the same.

While several injection locking mechanisms are available in the literature, using either active or passive components, most are explicit and implemented with dedicated components to ensure strong coupling, raising the overall power consumption and circuit area. In our circuit, we built upon the results obtained in [2], while further improving the PN and consumption by means of stacking more oscillators. The principle of injection lock is conceptually simple: by stacking several identical ring oscillators, which use the same current, a uniform voltage division is achieved between these oscillators, creating virtual grounds; each inverter peaks the supply current when switches; the current drawn from one inverter affects all the others in the stack; the periodic perturbations result is frequency lock between the ring oscillators and, consequently, an improvement in the overall PN.

TABLE I
Difference in performance of 1–4 oscillators.

Stack	V_{DD}	Power	PN@100kHz	PN@1MHz
1	225 mV	94.7 nW	-82.6 dBc/Hz	-103.7 dBc/Hz
2	450 mV	172.5 nW	-85.6 dBc/Hz	-106.4 dBc/Hz
3	675 mV	245.5 nW	-87.9 dBc/Hz	-107.5 dBc/Hz
4	900 mV	327.5 nW	-88.2 dBc/Hz	-108.5 dBc/Hz

TABLE II
Variation in frequency and power with bias current I_1.

Bias current (I_1)	Frequency	Power
2.5 nA	3 MHz	65 nW
7.5 nA	5 MHz	128 nW
15 nA	7.5 MHz	209 nW
40 nA	10 MHz	328 nW

In order to compare PN gains, we tested a single ring oscillator with a V_{DD} of 225 mV (which is the same available potential difference when four oscillators are stacked with 0.9 V of total supply voltage) to obtain a 10 MHz oscillation frequency. Also, we followed a similar approach for two and three stacked oscillators, maintaining 225 mV between the supply rails of each oscillator. The results are shown in Table I. It becomes clear that PN improves approximately −3 dBc/Hz when the number of stacked oscillators doubles. Comparing the single ring oscillator operating at 10 MHz with the stack of four, we obtain a PN improvement of almost −6 dBc/Hz.

Another interesting feature of the oscillator core is the possibility to tune the oscillation frequency without compromising the locking mechanism. By adding a current mirror to the stack of oscillators ($P_{1,2}$ in Fig. 2), we obtain an ICO which is tuned by I_1, providing a tuning range of 3 MHz–10 MHz. Table II presents the frequency and power consumption for several values of I_1, and in Fig. 5 we present the corresponding PN curves.

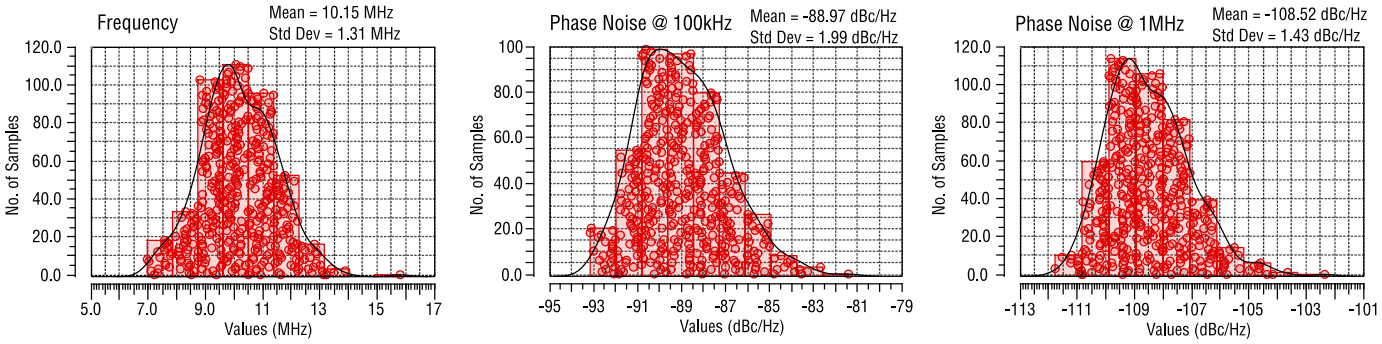

Fig. 3. Results of the Monte Carlo simulation for frequency and PN at 100 kHz and 1 MHz of offset.

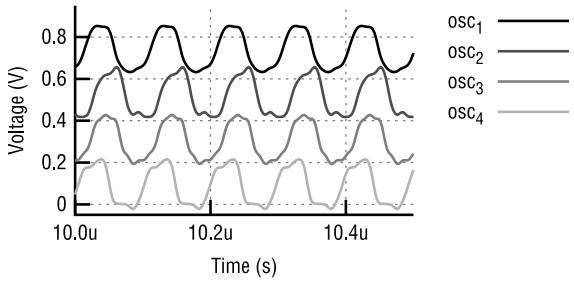

Fig. 4. Output voltages of the four stacked ring oscillators.

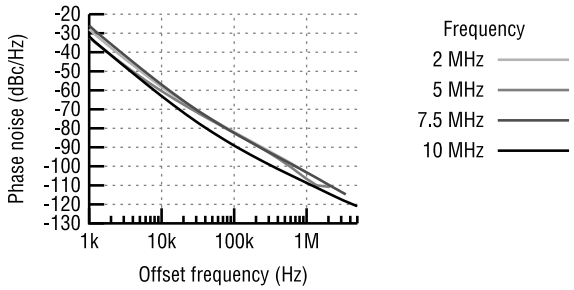

Fig. 5. PN for the oscillator tuned to various frequencies.

In the proposed approach, some attention must be drawn on the variability of the inverters. As the locking mechanism is only possible with similar values of t_d in the ring, excessive mismatch may compromise the injection lock. An oscillator using minimum inverters leads to almost 20% of frequency variation (standard deviation) which causes the oscillator to lose lock in many cases. Thus, larger transistors are required, and in this work we employed W_p = 7 µm, W_n = 6.8 µm and $L_{n,p}$ = 800 nm. The results of a Monte Carlo analysis are presented in Fig. 3. By implementing the inverters with larger dimensions, the standard deviation on the frequency drops to approximatelly 10%, while the frequency lock is achieved in all cases. The results of PN for 100 kHz and 1 MHz are also shown in Fig. 3.

IV. Duty-Cycle Calibrated Level Shifter

In order for the output of this circuit to be useful in the context of digital or mixed-signal circuits, a level shifter circuit must be employed. A regular level shifter converts a digital signal that swings from 0 to a low voltage V_{DDL} into a signal that swings between 0–V_{DDH}. This poses a few challenges when V_{DDL} and V_{DDH} are too far apart. In this work, we exploit the fact that many outputs are available, i.e. osc_{1-4}. Since the output of osc_2 is centered at ~537 mV, which is close to $V_{DD}/2$, we may use this signal to drive a simple inverter with sufficient voltage gain, which recovers the signal to V_{DD} easily. On the other hand, PVT variations would affect the threshold of such an inverter, and some sort of mechanism to adjust this threshold to the correct value must be employed. Thus, we employ a current-starved inverter together with a low-pass filter with a low-cutoff frequency, which outputs a voltage signal proportional to the duty-cycle, as a fraction of V_{DD}. This voltage signal is applied to an EA that is referenced to $V_{DD}/2$. The output of the EA controls the threshold of the inverter, guaranteeing a duty-cycle close to 50%, independently of PVT. The subcircuits are explained below.

A. Low-pass Filter

To obtain an RC filter with sufficiently low frequency poles for our application, very large values of capacitance and/or resistance must be used, which would result in a large circuit area if implemented with integrated passives. On the other hand, such an RC filter may be developed within a reasonable area if we employ MOSCAPs and MOS pseudo-resistors (PR), which can emulate resistors with giga or tera ohms [9]. PRs are known for being nonlinear resistors, in the sense that their emulated resistance largely depends on the voltage at its terminals, i.e. a nonlinear $R(V)$ curve. Different topologies have been explored to decrease this non-linearity [10], by stacking a different numbers of MOS and introducing feedback systems that compensate for the varying voltage. In this work, we propose a distributed filter, i.e. MOSCAPs are inserted between several PRs (P_{12-18} and N_{5-7} in Fig. 2). This approach grants a main advantage: each individual filter (MOSCAP plus preceeding PR) stabilizes the voltage imposed to the following section, reducing the nonlinearity of the PRs. Additionally, a larger-order filtering is achieved with little impact on the circuit area, which helps reducing the ripples on the EA input. The cutoff frequency of this filter does not need to be accurate, but must be much lower than the output frequency of the oscillator, and we picked ~1 kHz for this design.

B. Error Amplifier

The EA (P_{7-9} and N_{1-2} in Fig. 2) used in the duty-cycle calibration circuit is a p-type differential pair with n-type active

TABLE III
COMPARISON TABLE

	[3]	[4]	[5]	[6]	[7]	[8]	This work
Process [nm]	65	65	65	65	180	65	130
Simulated/Measured	Measured	Measured	Measured	Measured	Measured	Measured	Simulated
Topology	Relaxation	Relaxation	Ring	Relaxation	Ring	Wien bridge	Ring
Supply voltage [V]	0.35	1.2	0.3	1.2	1.2	1.2	0.9
Frequency [MHz]	18.2-29.2	12	12	12.6	1.4	6	10
Frequency Compensation	Yes	No	Yes	No	Yes	Yes	No
PN@100 kHz [dBc/Hz]	N/A	N/A	-83.86	-101	-75.8	-94.6	-88.8
PN@1 MHz [dBc/Hz]	-104.1	N/A	-105.69	N/A	N/A	N/A	-102.8
Power [μW]	17.8	84	5	98.4	0.615	66	0.7
FoM [dB]	-149.9@1M	-162@1M	-148.4@100k	-152.6@100k	-131@100k	-142@100k	-154@1M / -160@100k

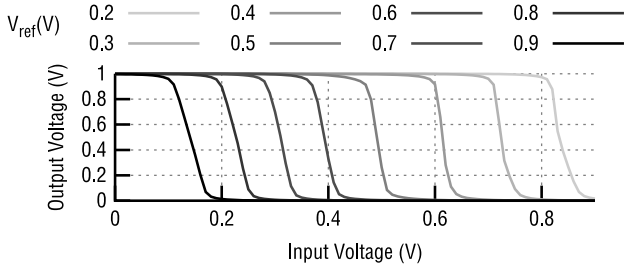

Fig. 6. Output vs. input characteristic of the current-starved inverter with various values of V_{ref}.

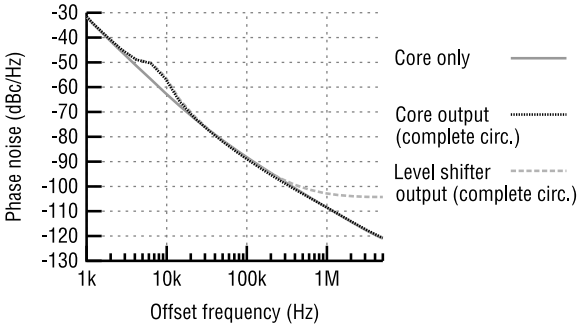

Fig. 7. PN of oscillator core only and complete circuit, measured at core output and level shifter output.

loads. This EA compares the output of the low-pass filter with a reference voltage of $V_{\text{DD}}/2$, generated by the voltage divider comprising P_{3-6} and bias the starved inverter accordingly. The biasing for P_7 also comes from this voltage divider. We sized the EA to achieve a DC gain of 37 dB with a bandwidth of 10 kHz, while consuming ∼10 nW. These specifications are sufficient to perform the relatively slow feedback loop. Additionally, the MOSCAP N_8 is added to the output of the amplifier to further reduce ripple and noise at the input of the starved inverter.

C. Starved Inverter with Reconfigurable Threshold

In order to adjust the duty-cycle of the oscillator, we used a starved inverter with a reconfigurable threshold (P_{10-11} and N_{3-4} in Fig. 2). This circuit is controlled by the output voltage of the EA, V_{ref}. The sensitivity to V_{ref} is shown in Fig. 6, that indicates a reconfigurable range of thresholds of ∼0.1–0.8 V.

D. Digital Buffer

Since the signal coming from the starved inverter is already rail-to-rail, a conventional digital buffer is used to drive the oscillator load. This buffer is able to drive capacitances up to 1 pF, but for the simulations presented in this paper, the load is only 1 fF.

V. Results

The complete oscillator uses 0.7 μW from a 0.9 V supply at 10 MHz, with a PN of −88.8 dBc/Hz at 100 kHz offset and −102.8 dBc/Hz at 1 MHz of offset. The PN curve is presented in Fig. 7 where we compare the difference between the PN of the oscillator core alone and the complete schematic, when measured at the oscillator core output and the level shifter output. By inspecting these curves, we conclude that the level shifter affects the PN at low frequencies (3 to 10 kHz), and raises the thermal noise level for over 1 MHz. A comparison with oscillators with similar specifications is presented in Table III. The figure of merit (FoM) used in the comparisons is expressed in (3).

$$\text{FoM} = \mathcal{L}(f_{\text{offset}}) + 20\log\left(\frac{f_{\text{offset}}}{f_1}\right) + 10\log\left(\frac{P_{\text{DC}}}{1\text{ mW}}\right) \quad (3)$$

VI. Discussion and Conclusion

In this paper we propose a small-area, low-power oscillator topology and a level shifter with duty-cycle calibration. Also, a new RC filter employing PRs with distributed MOSCAPs with improved linearity and symmetry is presented. The oscillator achieves low oscillation frequencies through the usage of multiple injection-locked stacked ring oscillators improving simultaneously the PN by approximately −6 dBc/Hz. The resulting oscillator targets frequencies in the range of few MHz and, oscilatting at 10 MHz, achieves a PN of -88.8 dBc/Hz at 100 kHz and -102.8 dBc/Hz at 1 MHz of offset, while burning only 0.7 μW from a 0.9 V voltage supply. Comparison with the literature places this design among the state-of-the-art in terms of FoM for the targeted range of frequencies.

Acknowledgments

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