ISCAS 2020
2020 IEEE International Symposium on Circuits and Systems
Virtual, October 10-21, 2020

IEEE CAS

Low-Power SAR ADC techniques and applications

Pieter Harpe

Eindhoven University of Technology

2020 IEEE International Symposium on Circuits and Systems
Virtual, October 10-21, 2020

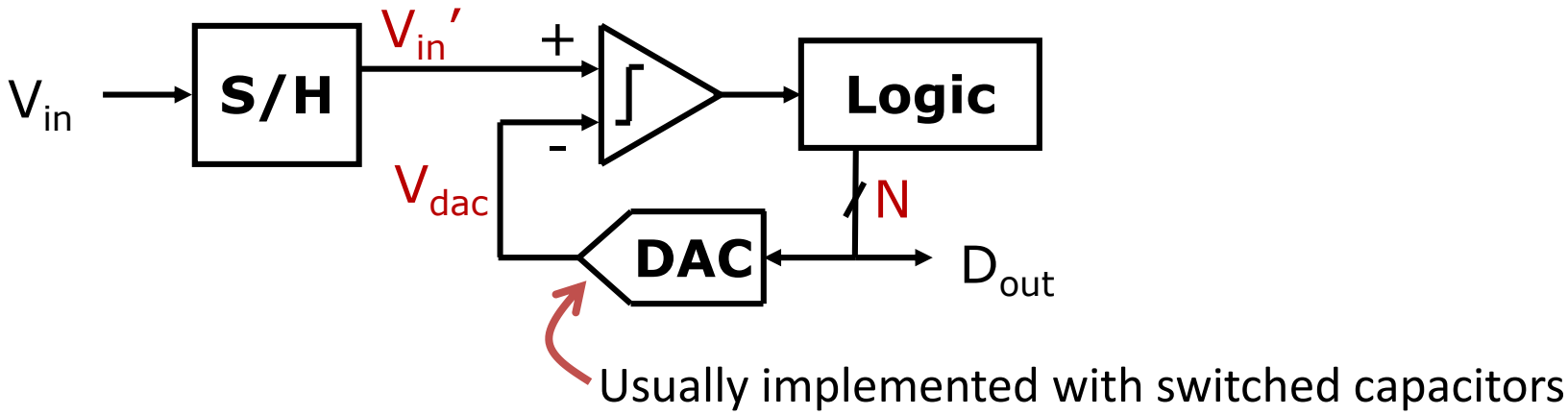
TU/e EINDHOVEN UNIVERSITY OF TECHNOLOGY

IC INTEGRATED CIRCUITS

Outline

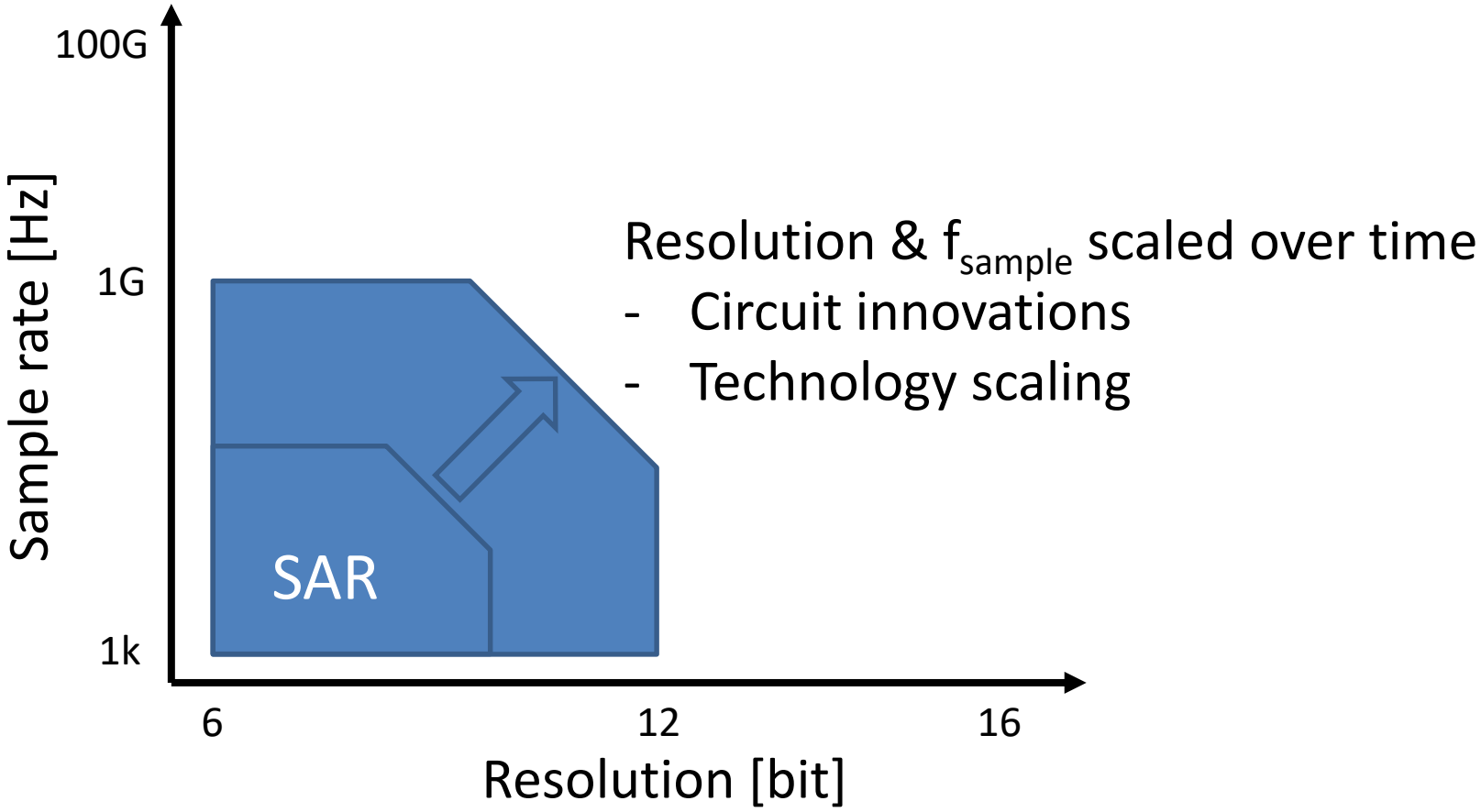
- Introduction, trends & applications
- Low-speed vs high-speed SAR ADCs
- Techniques for power-efficient SAR ADCs
- Application examples
- Limitations and future trends
- Conclusion

SAR ADC introduction



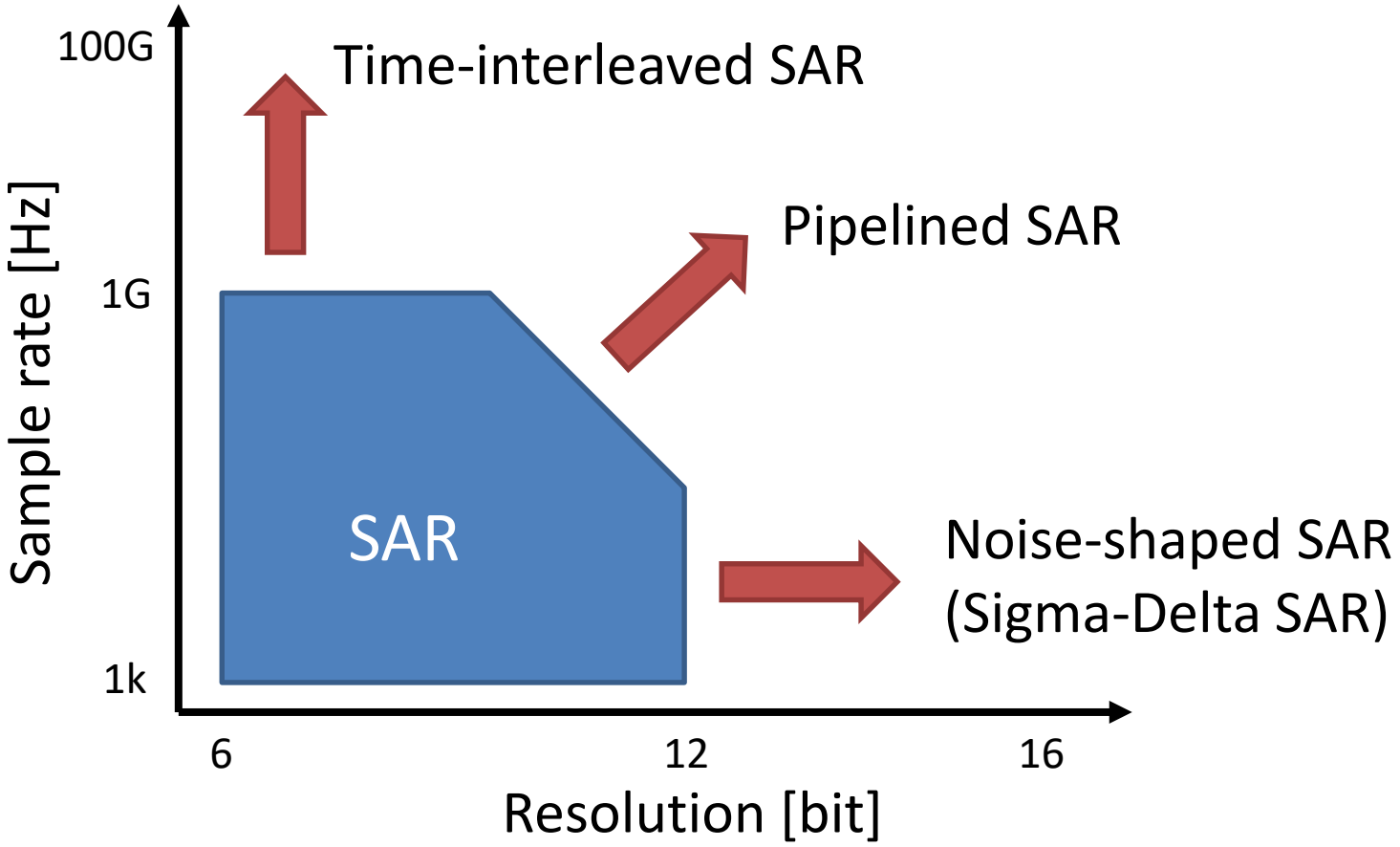
- Efficient algorithm (binary search)
- Simple circuit design
- Scales well with technology, VDD, f_{sample}
- By default no calibration/trimming since there are no critical bias currents/RC constants/offsets

SAR ADC performance area



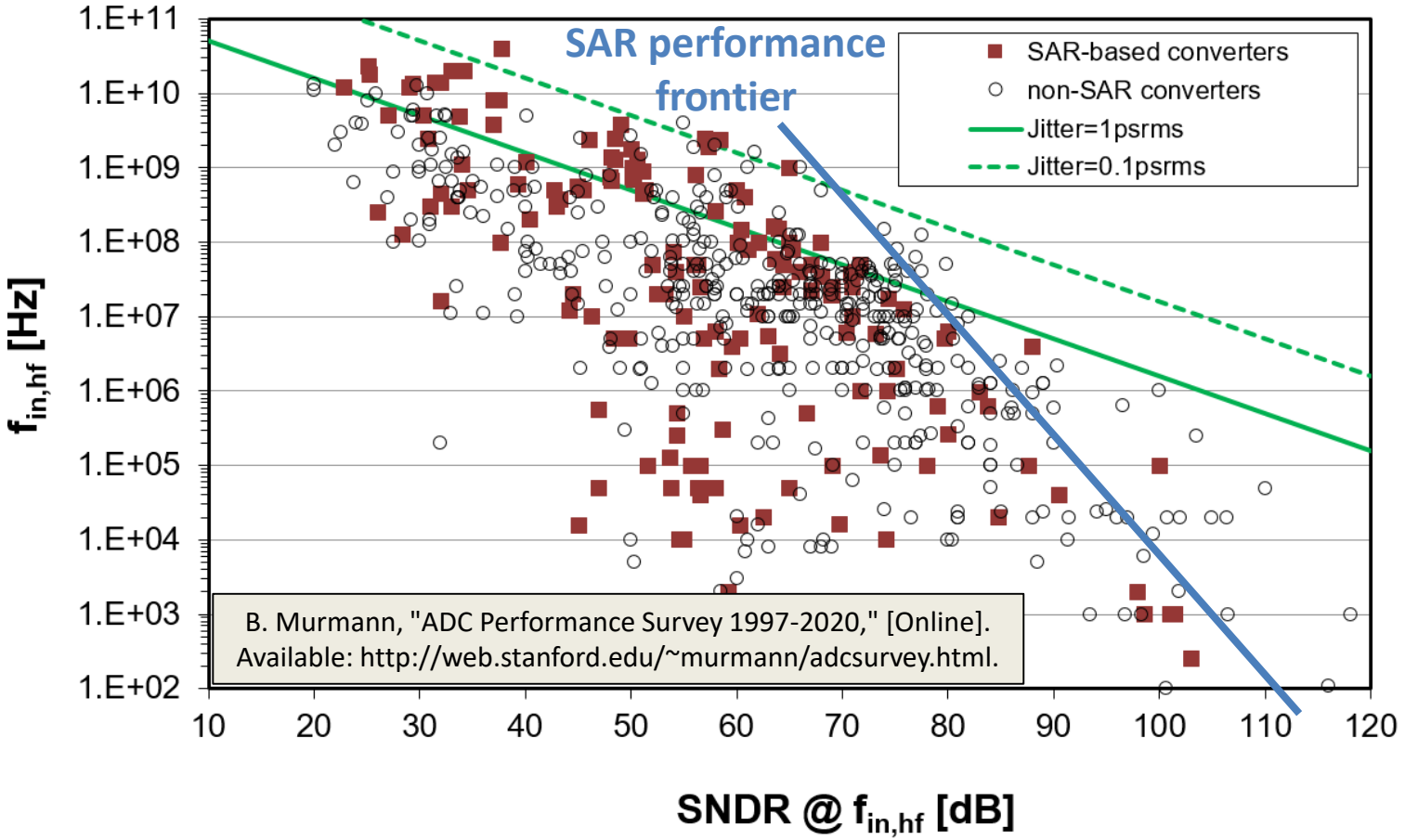
- SAR ADCs became of interest for power constrained applications: battery powered & wearable systems, IoT

SAR ADC performance area



- **SAR-*only*** ADCs for medium speed/resolution applications
- SAR performance frontier uses **SAR-*based*** ADCs

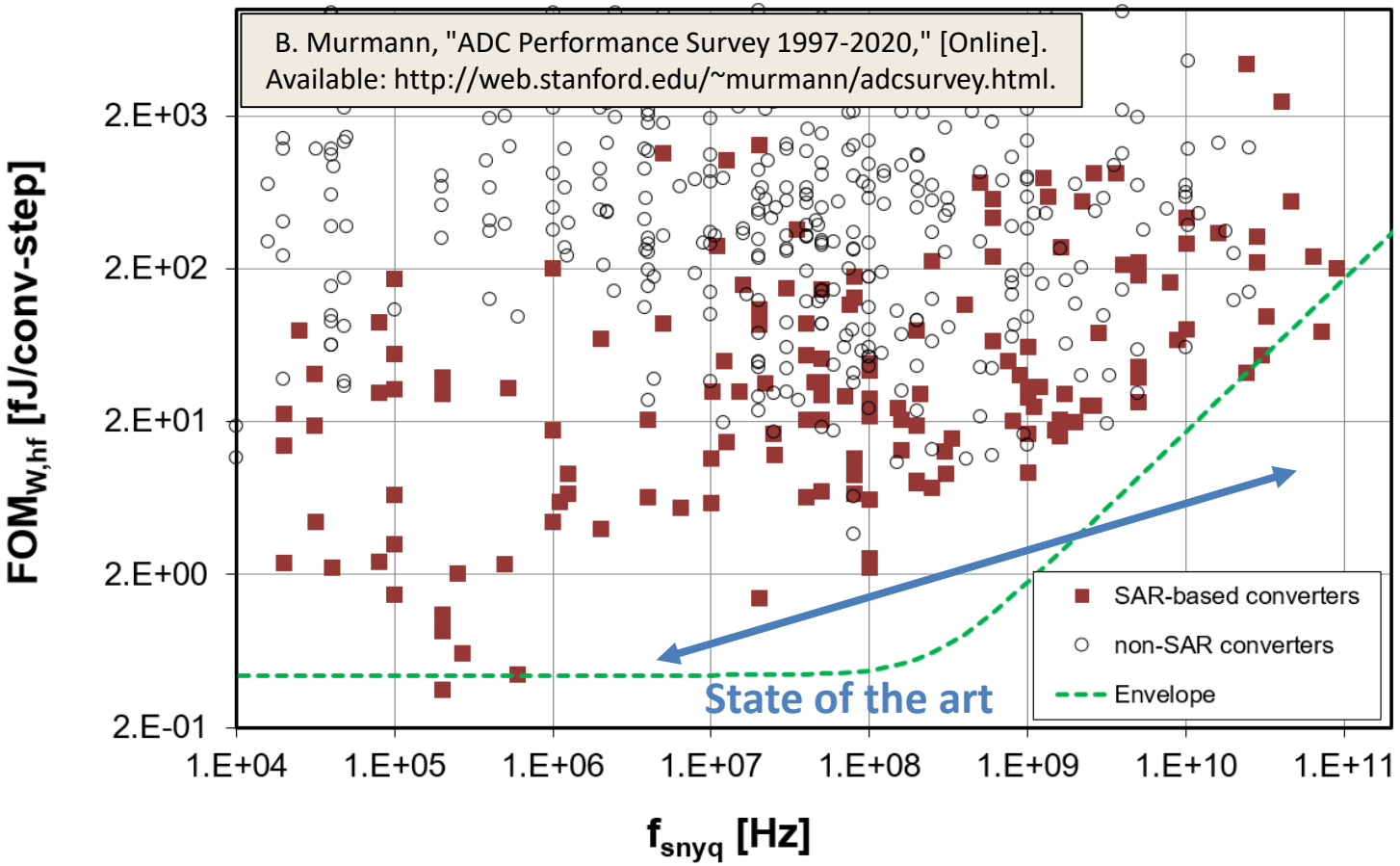
ADC trends: frequency vs SNDR



- SAR-based ADCs cover almost every application

  Except highest resolutions

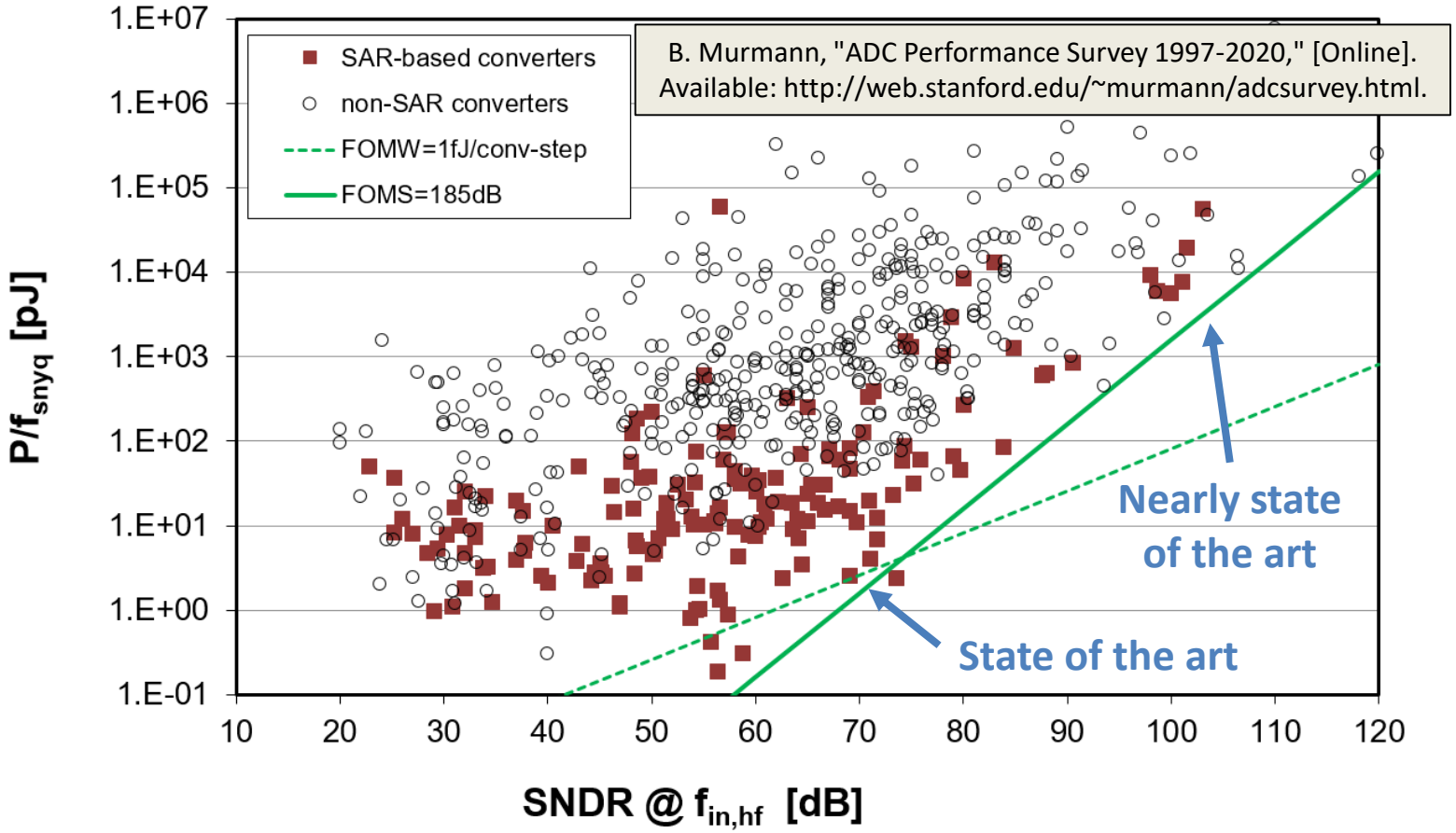
ADC trends: efficiency vs f_{sample}



- SAR-based ADCs are highly efficient

  For any speed of operation

ADC trends: efficiency vs SNDR



- SAR-based ADCs are highly efficient

  Especially for <70dB SNDR, but gradually also for >70dB SNDR

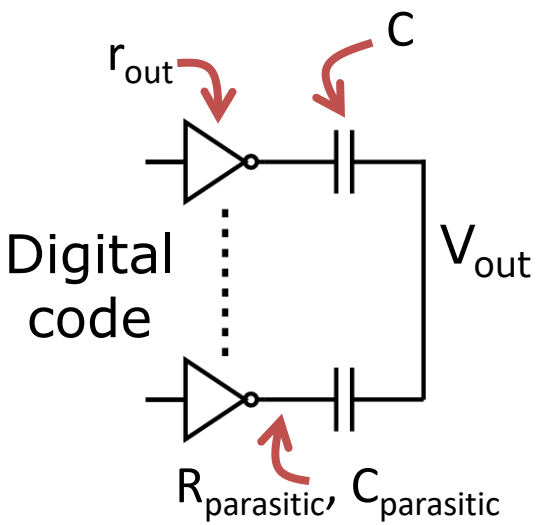
Low-speed vs high-speed design

Low speed ADC

Optimize efficiency

- kT/C (noise)
- C (matching)
- $\alpha \cdot CV^2$ (energy)
- $C_{parasitic}$ (energy)

DAC



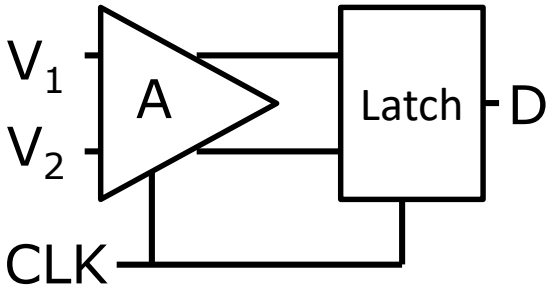
High speed ADC

Optimize BW & timing

- RC constants: r_{out}, C, $R_{parasitic}$, $C_{parasitic}$ (delay)
- Sampling switch timing (jitter/skew)

- Noise
- Energy

Comparator



- Delay

Low-speed vs high-speed design

Low speed ADC

- Parasitic C's: increase energy consumption

Layout

High speed ADC

- Parasitic R & C's: delay → speed limit

- Lower VDD ☺
- Smaller devices ☺
- More leakage ☹

Technology scaling

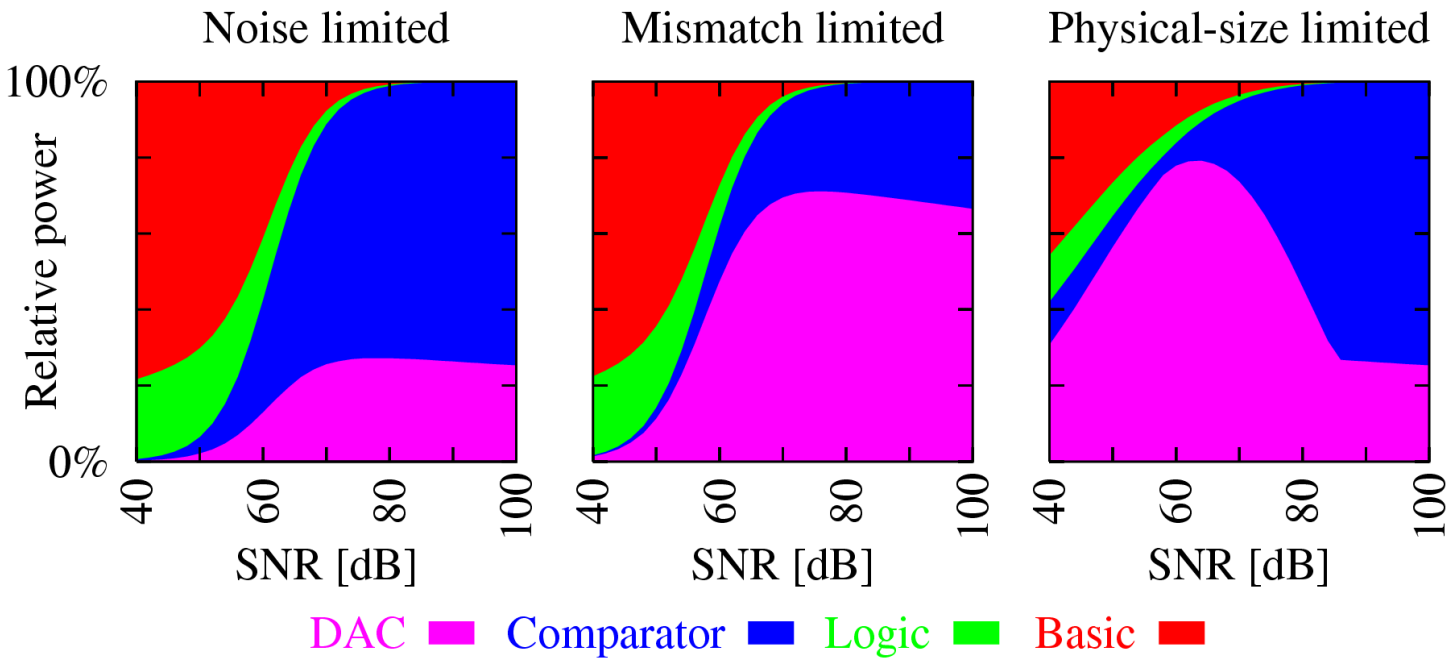
- Higher intrinsic speed ☺

Outline

- Introduction, trends & applications
- Low-speed vs high-speed SAR ADCs
- Techniques for power-efficient SAR ADCs
- Application examples
- Limitations and future trends
- Conclusion

Techniques for power-efficiency

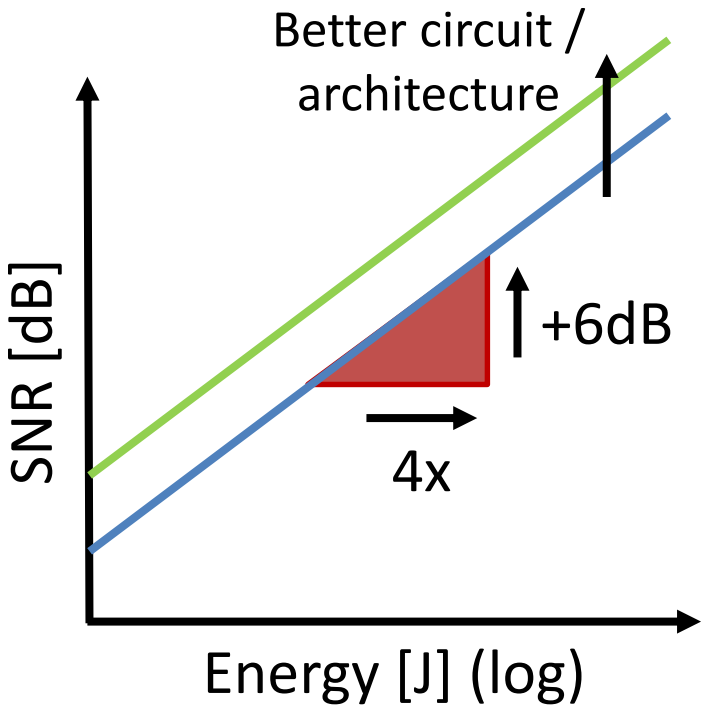
- Power efficiency: SNDR vs energy consumption
  - Noise & linearity versus energy consumption
- What is the main bottleneck?



P. Harpe, et al., "Low-power SAR ADCs: trends, examples and future," IEEE ESSCIRC, 2019.

Noise improvement

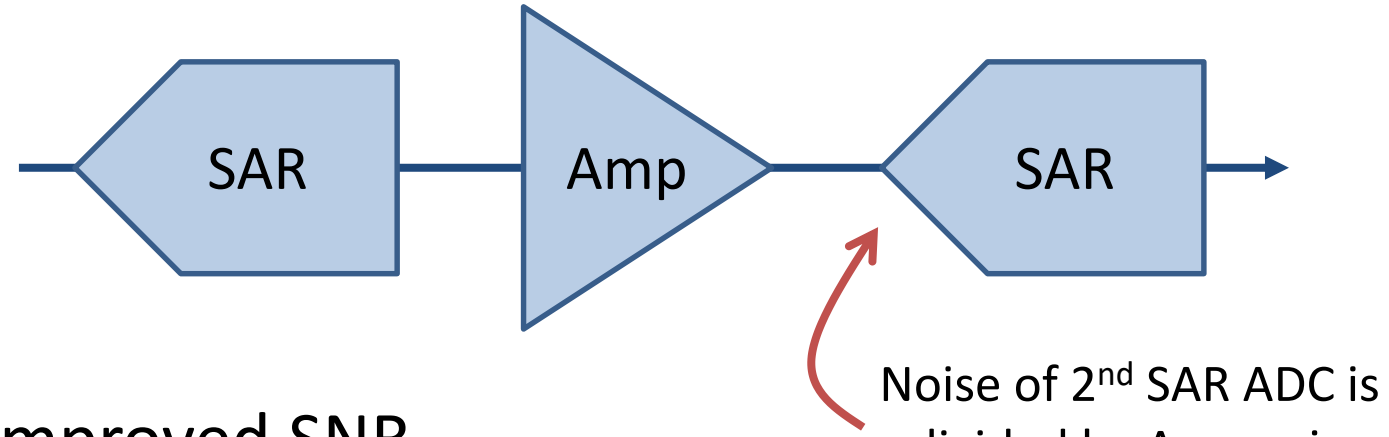
- Fundamental trade-off energy – noise
- Example for SC-DAC:
  - Energy $\propto CV^2$
  - SNR $\propto V^2 / (kT/C)$
  - Efficiency (Energy/SNR) $\propto kT$



- More efficient circuit or architecture
  - Amplification
  - Averaging
  - Filtering

Noise improvement – Amplification (1)

- Pipelined SAR ADC

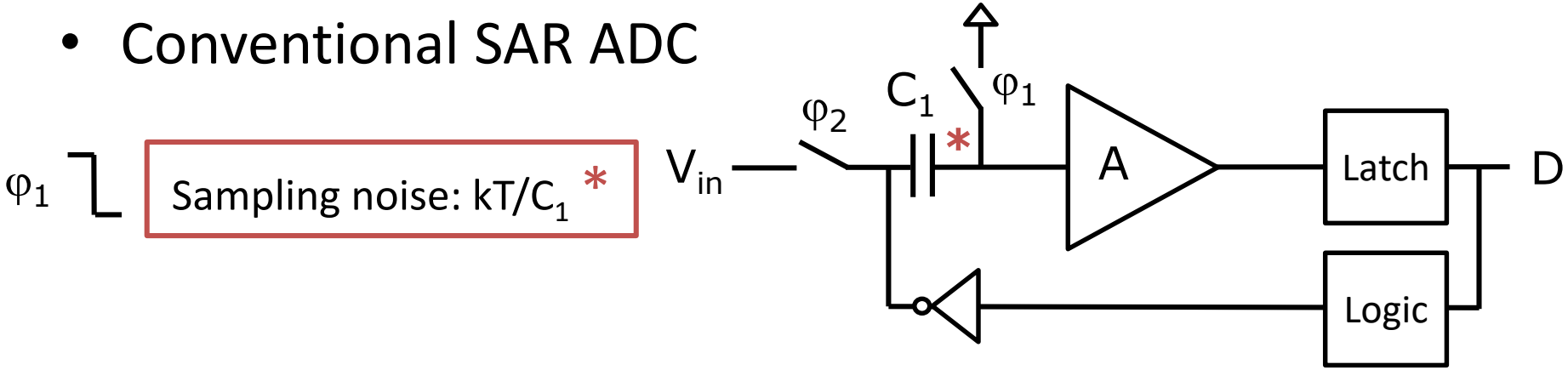


  - Improved SNR
  - Increased throughput rate
- Efficient amplifier required
  - May need offset/gain/linearity calibration

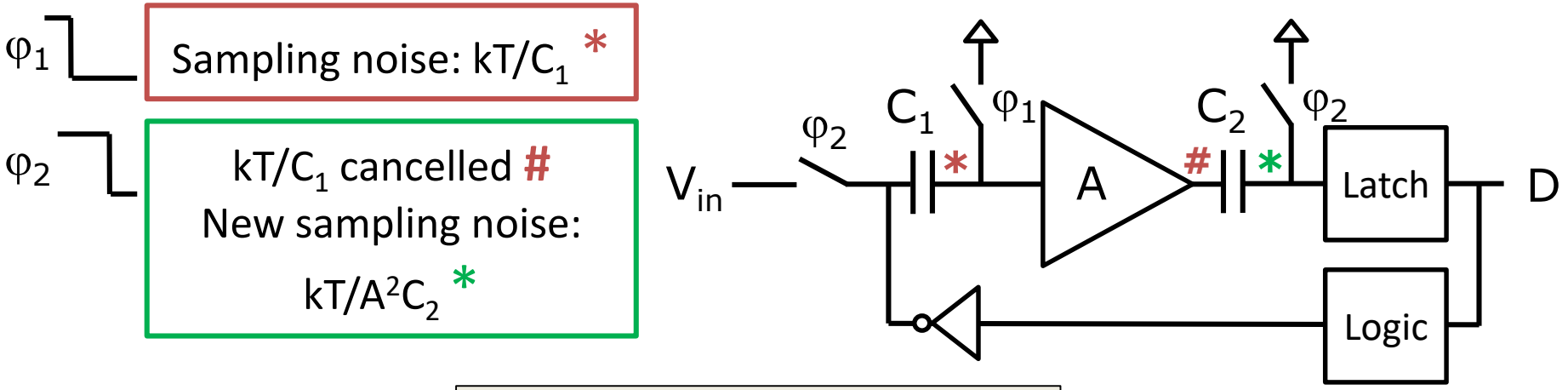
K. Bult, et al., "High-Efficiency Residue Amplifiers," in Low-Power Analog Techniques, Sensors for Mobile Devices, and Energy Efficient Amplifiers - Advances in Analog Circuit Design 2018, Springer.

Noise improvement – Amplification (2)

- Conventional SAR ADC

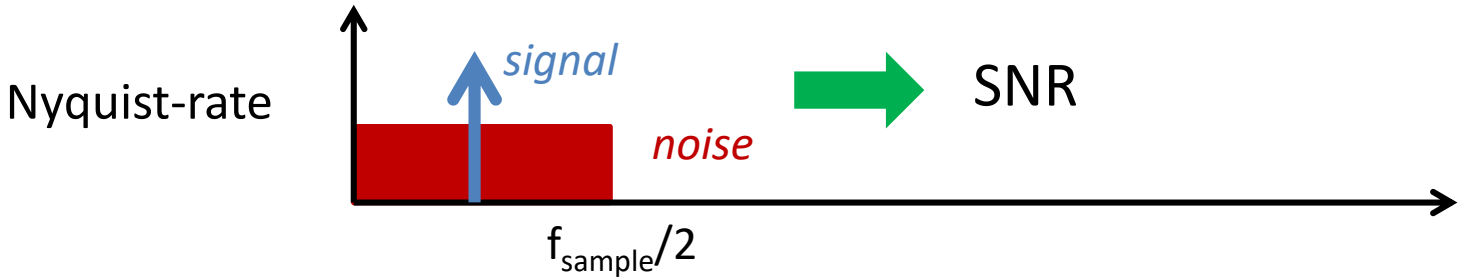


- SAR ADC with kT/C noise cancellation

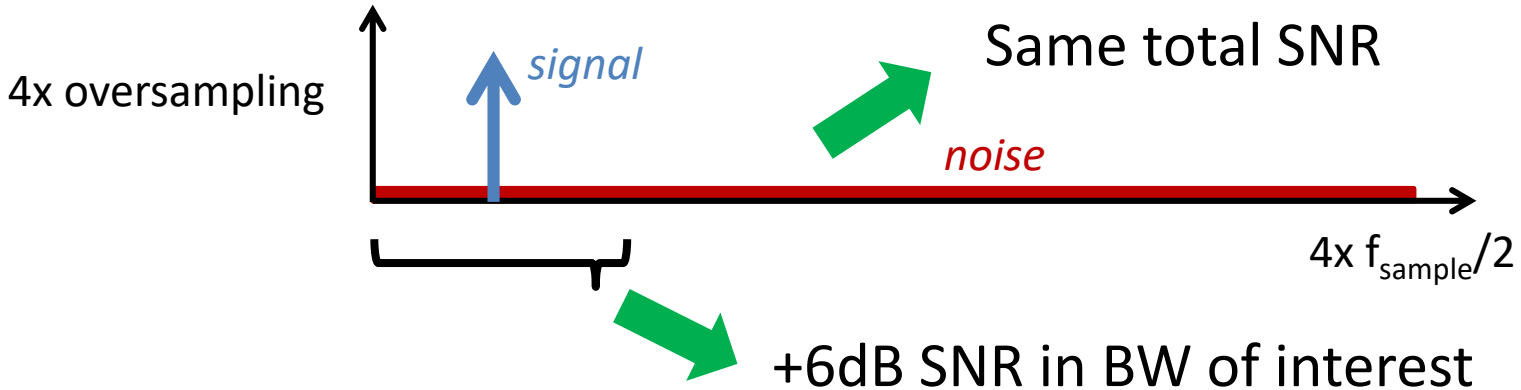


J. Liu, et al., "A 13b 0.005mm² 40MS/s SAR ADC with kT/C Noise Cancellation," IEEE ISSCC 2020.

Noise improvement – Averaging (1)

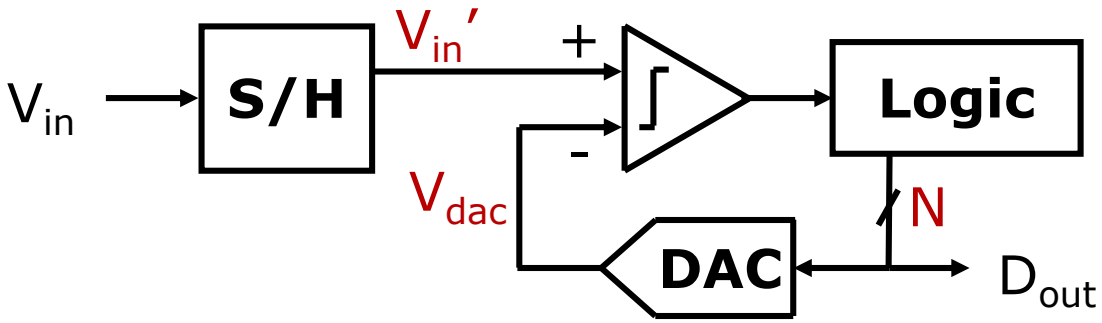


- Oversampling



- Every 4x OSR (≈4x power)→ +6dB SNR → Constant efficiency

Noise improvement – Averaging (2)



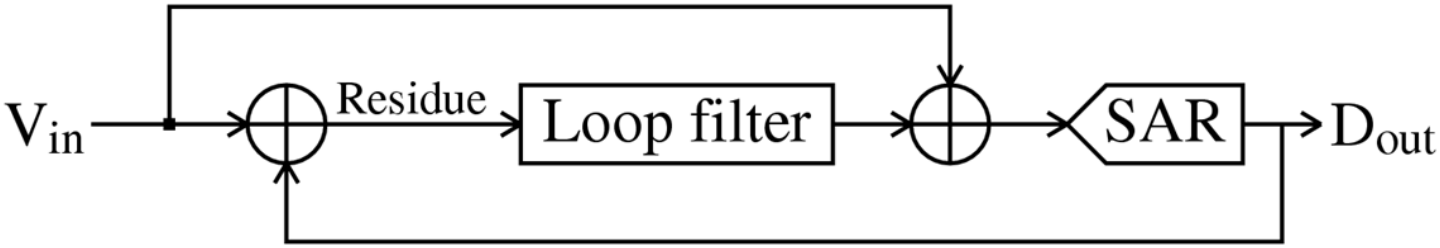
- # comparator decisions: N x 1
- Repeat same decision and take majority vote → averages comparator noise. E.g.: 11001 → 1
  - When $|V_{in}' - V_{dac}|$ large: 1 decision reliable enough — 80% N x 1
  - When $|V_{in}' - V_{dac}|$ small: vote on multiple decisions — 20% N x 5

Comparator SNR +6dB with less than 2x power ← 1.8 x N

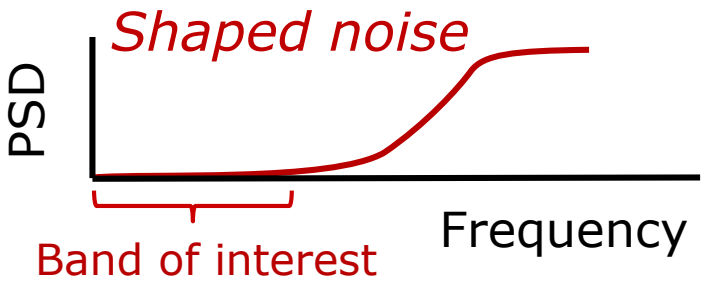
P. Harpe, et al., "A 10b/12b 40 kS/s SAR ADC With Data-Driven Noise Reduction Achieving up to 10.1b ENOB at 2.2 fJ/Conversion-Step," IEEE JSSC, Vol. 48, No. 12, 2013.

Noise improvement – Filtering (1)

- Noise-shaping SAR: Oversampling + noise-shaping
  - Residue voltage of SAR ADC (available @ DAC after conv.)
  - Integrate this (loop filter) and add to input signal

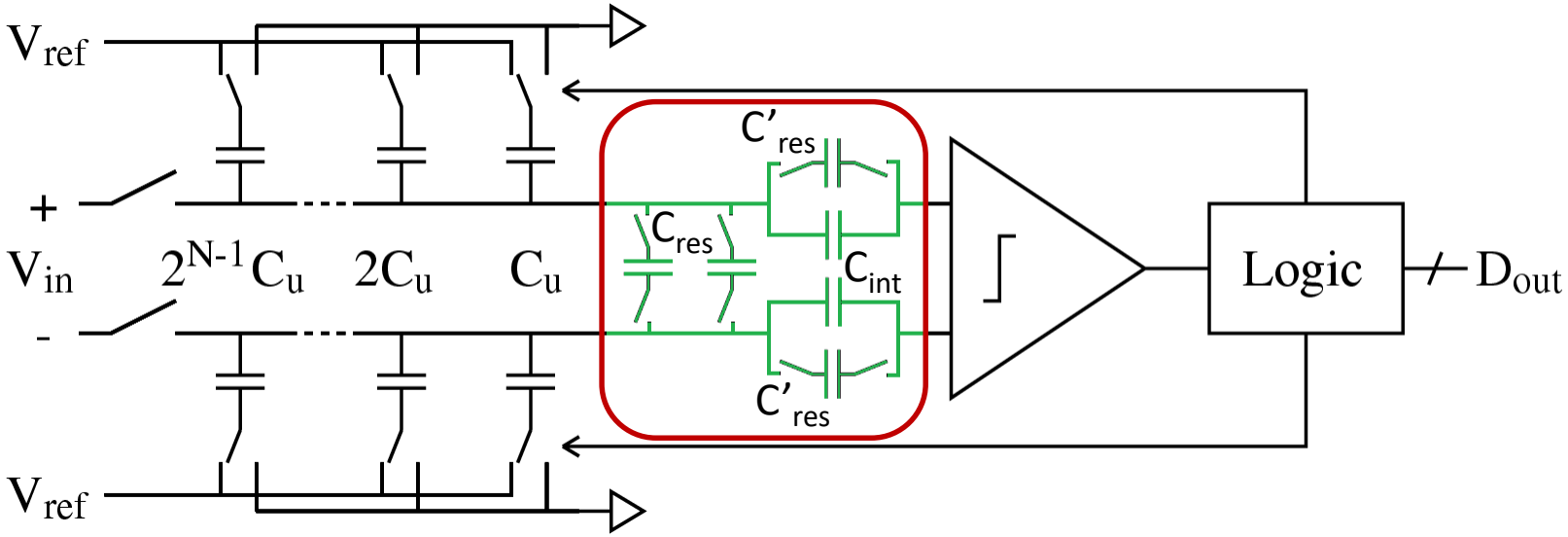


- Result: noise-shaping



Typical values	NS-SAR	SDM
$N_{quantizer}$	6 .. 10b	1 .. 4b
OSR	4x … 16x	16x … >100x
Filter order	1^{st} .. 2^{nd}	2^{nd} .. 4^{th}

Noise improvement – Filtering (2)

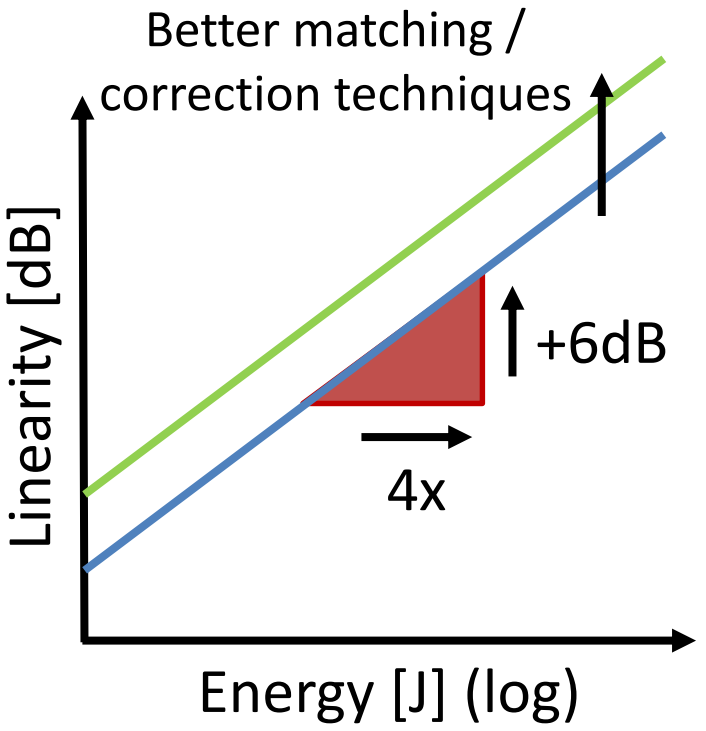


1. After SAR conversion, sample $V_{residue}$ on C_{res} capacitors
2. Flip position of C_{res} and C'_{res} capacitors
   - Voltage on C_{res} is averaged with voltage on C_{int} → Integration
   - C_{int} is in series with the DAC, so its value is added to the next sample

Y-Z Lin, et al., "A 40MHz-BW 320MS/s Passive Noise-Shaping SAR ADC with Passive Signal-Residue Summation in 14nm FinFET," IEEE ISSCC 2019.

Linearity improvement

- Trade-off caused by DAC element mismatch
- Example for SC-DAC:
  - Mismatch $\sigma^2 \propto 1 / A \propto 1 / C$
  - +6dB linearity → ½ x σ → 4x A and 4x C, so 4x energy



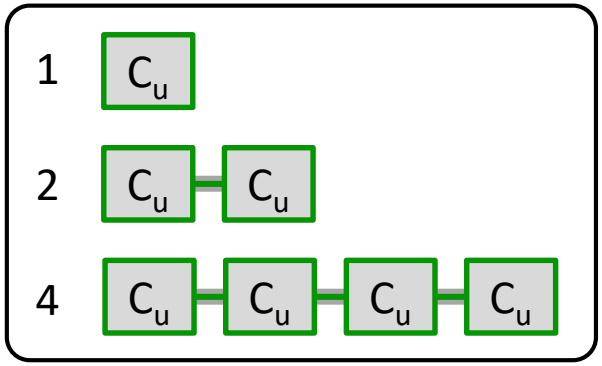
- Linearity enhancement techniques
  - Improve matching of DAC elements
  - Calibration
  - Mismatch error shaping (MES)

Linearity improvement – Capacitor design (1)

- Binary code

	LSB			MSB
Digital weight	1	2	4	8
Analog weight	$1+\varepsilon_1$	$2+\varepsilon_2$	$4+\varepsilon_4$	$8+\varepsilon_8$

- Accurate matching: unit elements



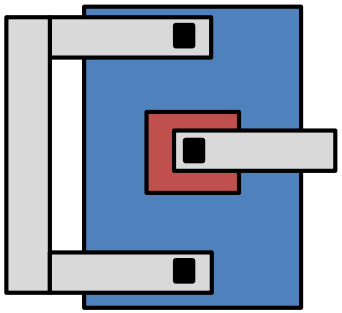
- Many elements ☹
- Requires small C_u with good σ

Capacitor values (kT/C limit @$1V_{pp}$)

# bits N	2^N	$C_s = 2^N C_u$	C_u
6	64	0.2fF	3aF
8	256	3.3fF	13aF
10	1024	52fF	51aF
12	4096	0.8pF	0.2fF
14	16384	13pF	0.8fF
16	65536	0.2nF	3.2fF

Linearity improvement – Capacitor design (2)

- Capacitor implementations

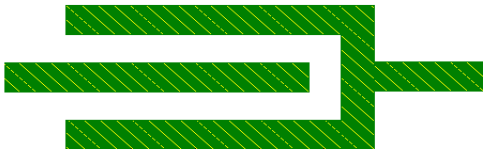


MIMCAP

Area inefficient

C_{min} usually > 2fF

1 design parameter (A), which sets C and σ



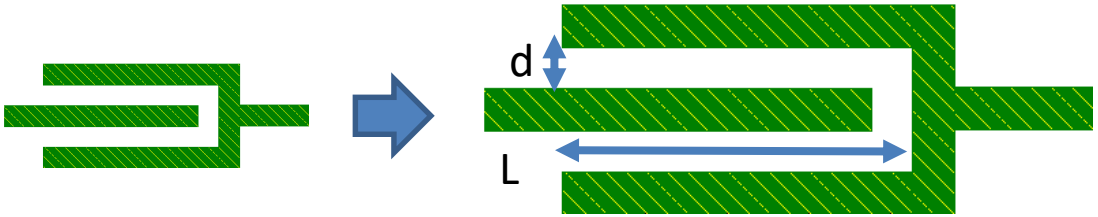
MOMCAP

Area efficient

C_{min} < 0.25fF

More design parameters (length, width, spacing, # layers)

Partial decoupling of A, C, and σ



Double space (d)

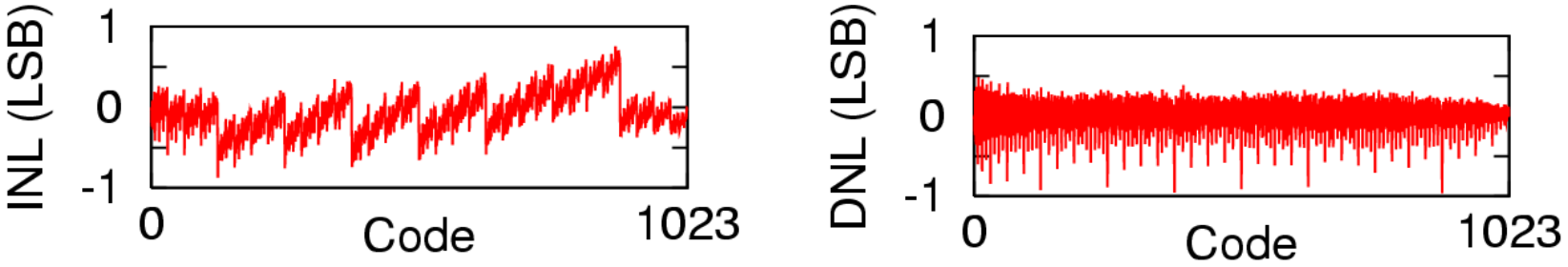
Double length (L)

→ Same C, larger A, better σ

P. Harpe, et al., "A 26μW 8bit 10MS/s Asynchronous SAR ADC for Low Energy Radios," IEEE JSSC, Vol. 47, No. 7, 2011.

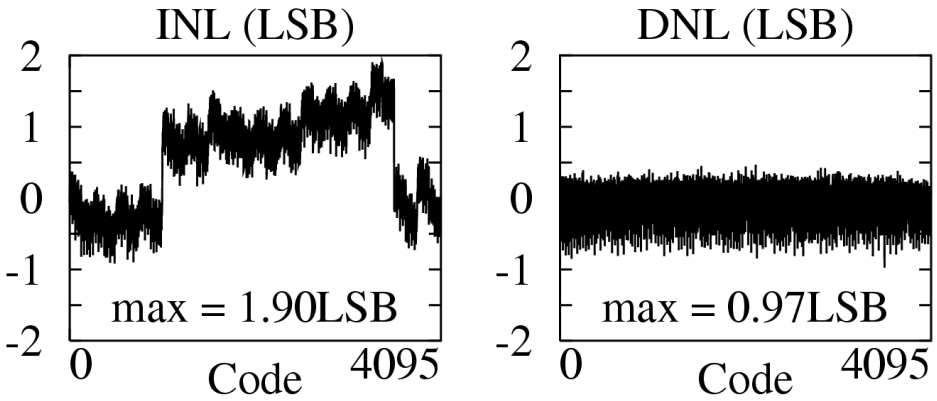
Linearity improvement – Capacitor design (3)

- Example: SAR ADCs in 65nm CMOS with C_u = 250aF
  - 10b ADC:



P. Harpe, et al., "A 3nW Signal Acquisition IC Integrating an Amplifier with 2.1 NEF and a 1.5fJ/conversion-step ADC," IEEE ISSCC, 2015.

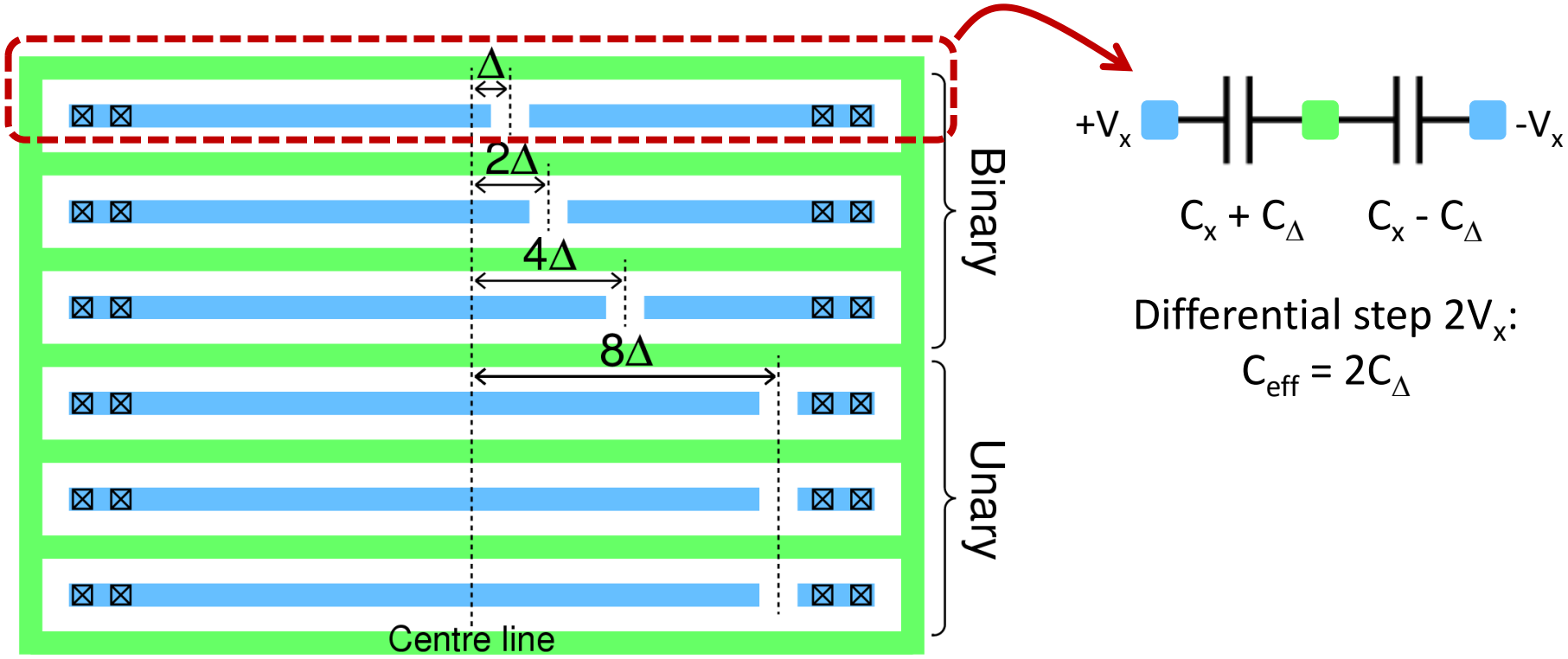
  - 12b ADC:



P. Harpe, et al., "A 10b/12b 40 kS/s SAR ADC With Data-Driven Noise Reduction Achieving up to 10.1b ENOB at 2.2 fJ/Conversion-Step," IEEE JSSC, Vol. 48, No. 12, 2013.

Linearity improvement – Capacitor design (4)

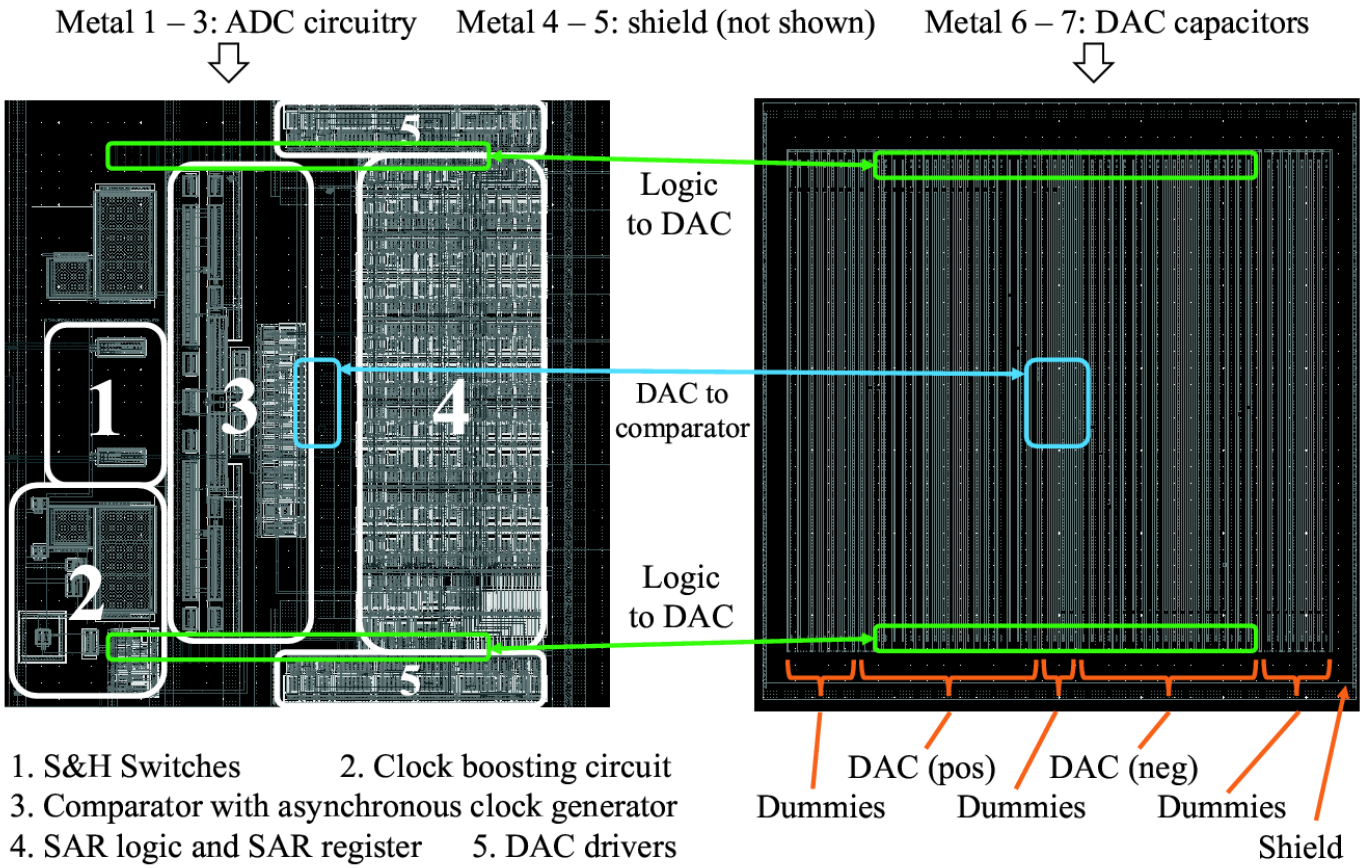
- Delta-length capacitors: smaller $C_{u,eff}$, compact, #elements is linear in N rather than 2^N



P. Harpe, "A Compact 10b SAR ADC with Unit-Length Capacitors and a Passive FIR Filter," IEEE JSSC, Vol. 54, No. 3, 2019.

Linearity improvement – Capacitor design (5)

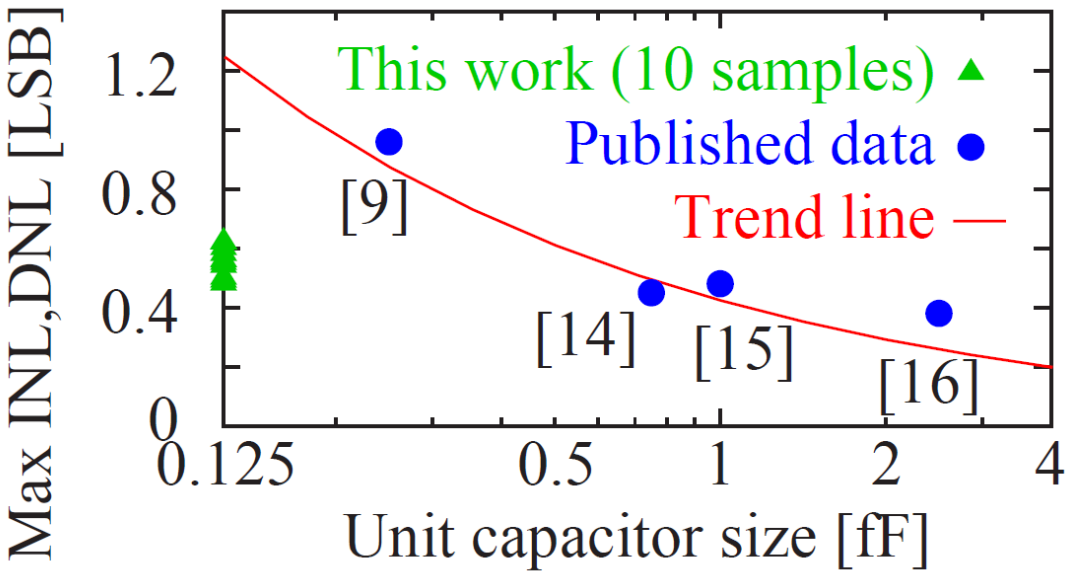
- Design example: 10b SAR ADC in 65nm CMOS



P. Harpe, "A Compact 10b SAR ADC with Unit-Length Capacitors and a Passive FIR Filter," IEEE JSSC, Vol. 54, No. 3, 2019.

Linearity improvement – Capacitor design (6)

- Design example: 10b SAR ADC in 65nm CMOS
  - C_u = 125aF, ADC size 36 x 36 μm
  - Small area, low power, good matching



Note: [9],[14-16] can be found in the paper below

P. Harpe, "A Compact 10b SAR ADC with Unit-Length Capacitors and a Passive FIR Filter," IEEE JSSC, Vol. 54, No. 3, 2019.

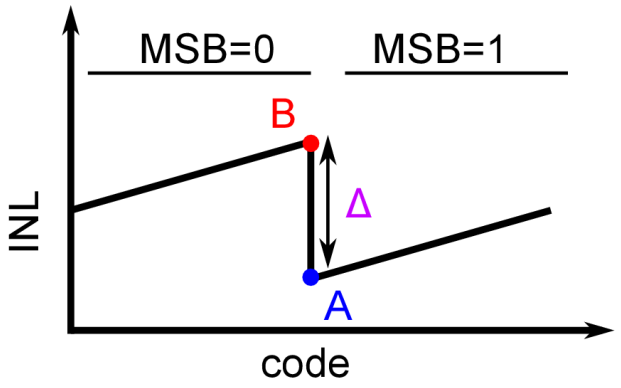
Linearity improvement – Calibration

	LSB			MSB
Digital weight	1	2	4	8
Analog weight	$1+\varepsilon_1$	$2+\varepsilon_2$	$4+\varepsilon_4$	$8+\varepsilon_8$

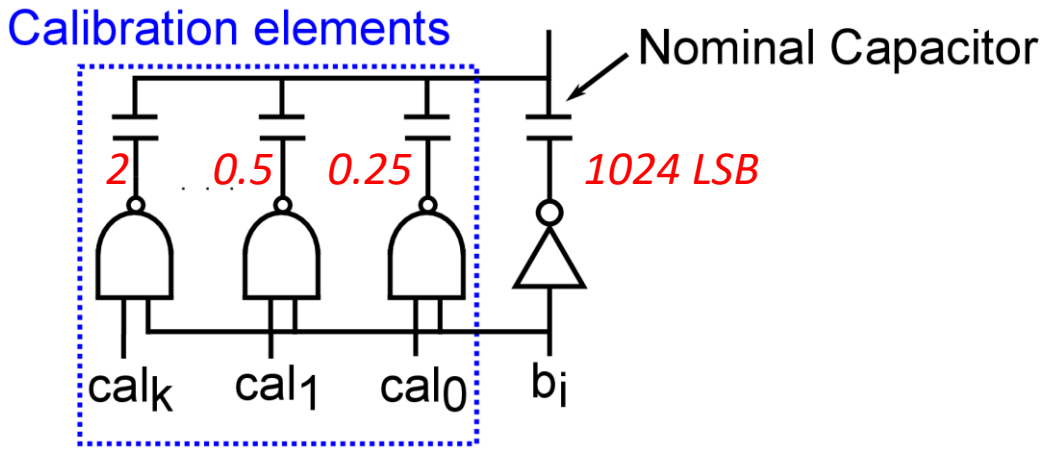
- Aim: rather than minimizing ε's a-priori, apply calibration afterwards to match analog and digital weights:
  - Step 1: acquire info about ε's after production
  - Step 2: correct weights so analog matches digital
    - Analog correction: tune ε's towards zero
    - Digital correction: tune digital weights towards ε's
  - Digital correction usually consumes more (high-res ADDers)
  - Analog correction is usually efficient (trim capacitors)

Linearity improvement – Calibration (1)

- Example: 13b SAR ADC with background calibration:
  - Digital detection
    - Mismatch shows at major code transitions in INL/DNL
    - If code B occurs, the ADC switches to A-1
    - Extra comparison reveals sign of Δ
    - Capacitor can be tuned towards zero error



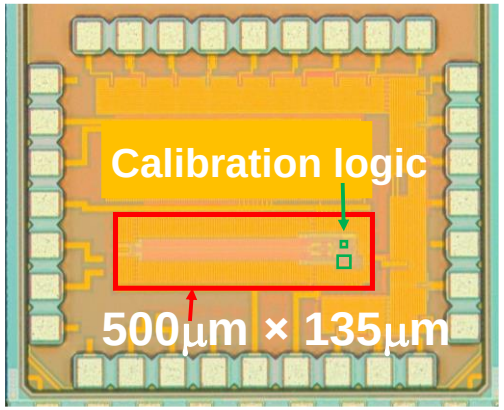
  - Analog correction

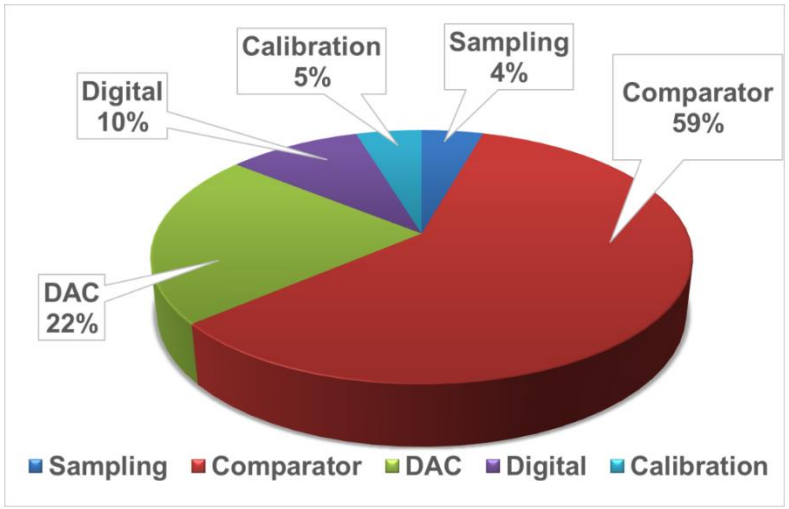


M. Ding, et al. "A 46µW 13b 6.4MS/s SAR ADC With Background Mismatch and Offset Calibration," IEEE JSSC, Vol. 52, No. 2, 2017.

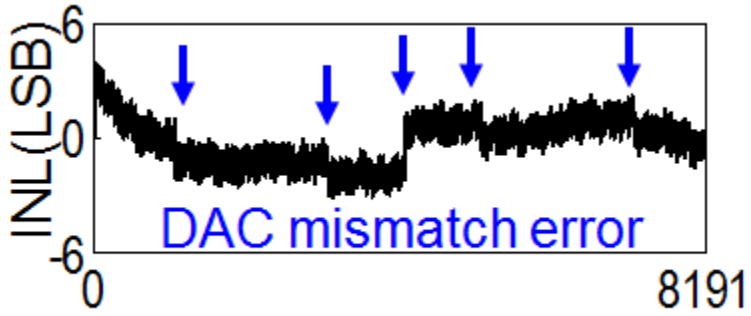
Linearity improvement – Calibration (2)

- Implemented in 40nm CMOS. Power and area overhead is low

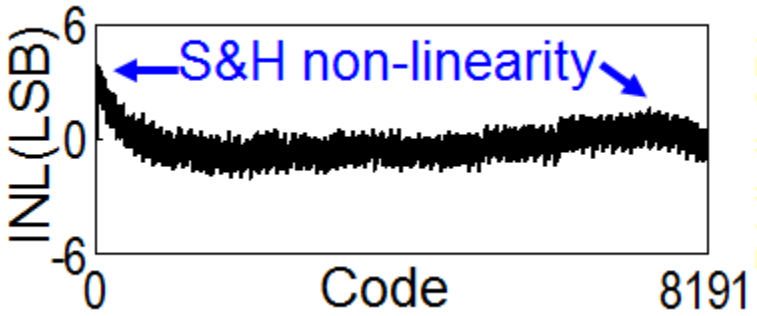




Before calibration



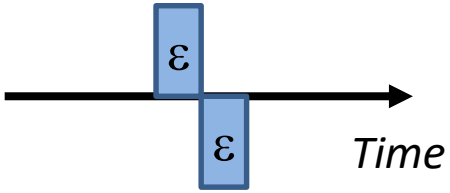
After calibration



M. Ding, et al. "A 46µW 13b 6.4MS/s SAR ADC With Background Mismatch and Offset Calibration," IEEE JSSC, Vol. 52, No. 2, 2017.

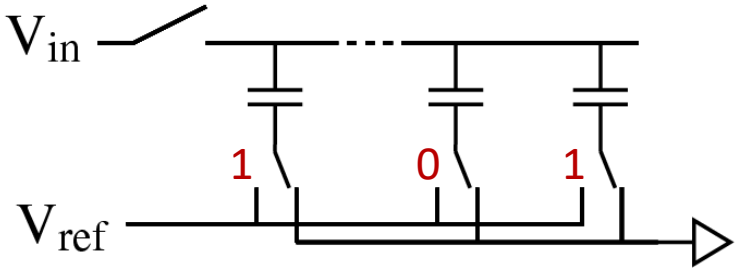
Linearity improvement – MES

- Noise shaping – Mismatch Error Shaping



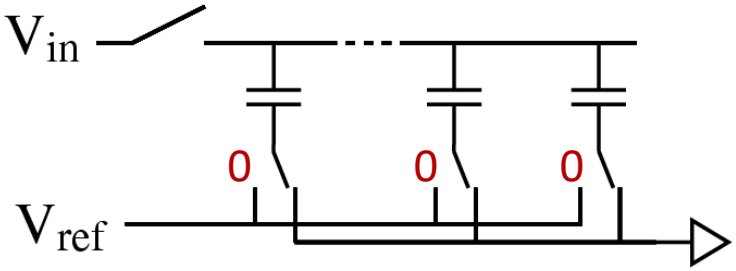
High-pass filter: $1 - z^{-1}$

MES SAR @ sampling phase



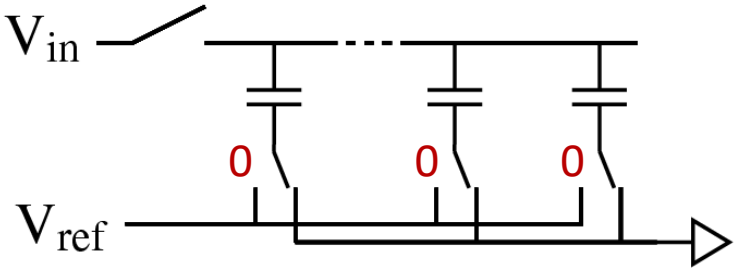
- DAC remains at previous code

Normal SAR @ sampling phase



- DAC reset to mid-scale
- No memory from prev. sample

MES SAR: DAC reset



- DAC reset to mid-scale
- previous code (and ε) subtracted

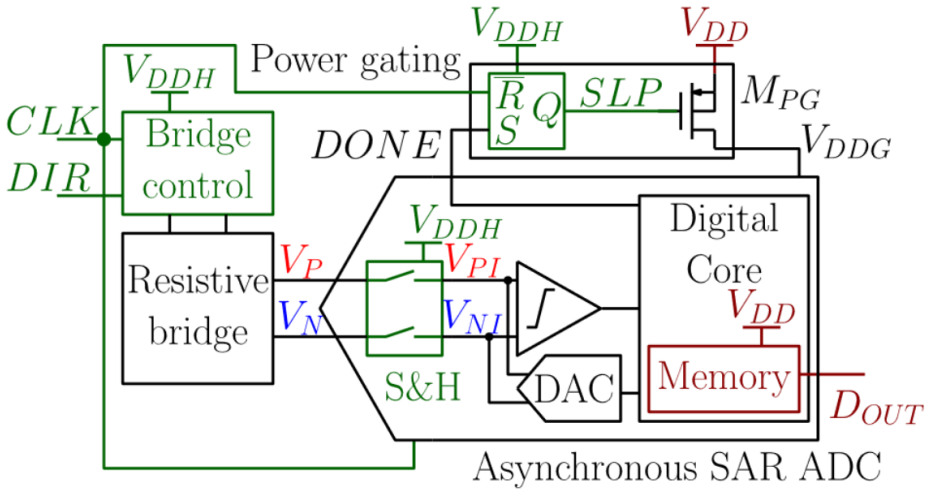
Y-S Shu, at al., "An Oversampling SAR ADC with DAC Mismatch Error Shaping Achieving 105dB SFDR and 101dB SNDR over 1kHz BW in 55nm CMOS," IEEE ISSCC 2016.

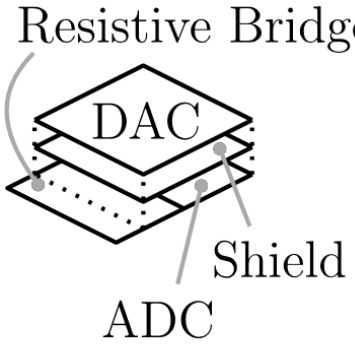
Outline

- Introduction, trends & applications
- Low-speed vs high-speed SAR ADCs
- Techniques for power-efficient SAR ADCs
- Application examples
- Limitations and future trends
- Conclusion

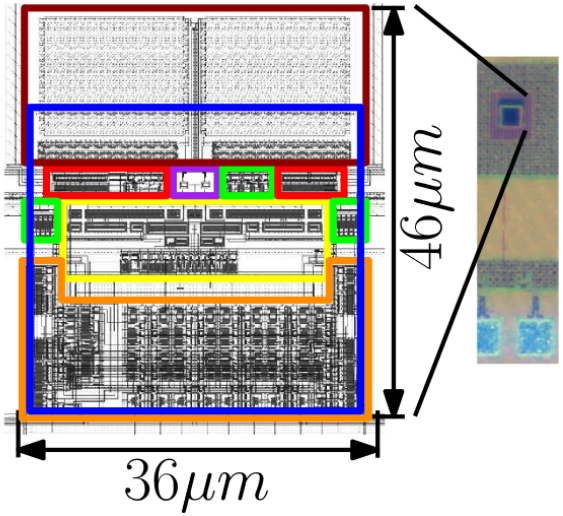
Power & Area-efficient sensors

- Power gated bridge & ADC
  - 2.18pJ/sensor reading
  - Power scaling vs speed
- Area-efficient ADC
  - 36 x 46 µm in 65nm CMOS



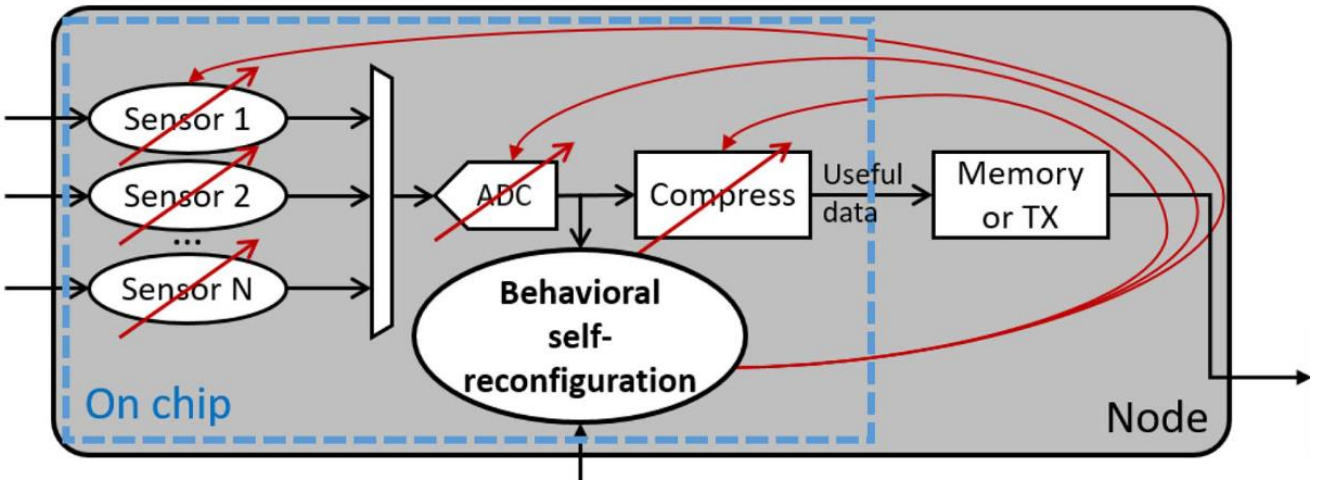


- Resistive bridge
- Bridge control
- Power gating
- Sample & hold
- Comparator
- Control logic
- DAC (Not shown)



K. Pelzers, et al., "A 2.18-pJ/conversion, 1656-µm² Temperature Sensor With a 0.61-pJ·K² FoM and 52-pW Stand-By Power," IEEE SSCL, Vol. 3, 2020.

Smart self-adaptive sensor SoC

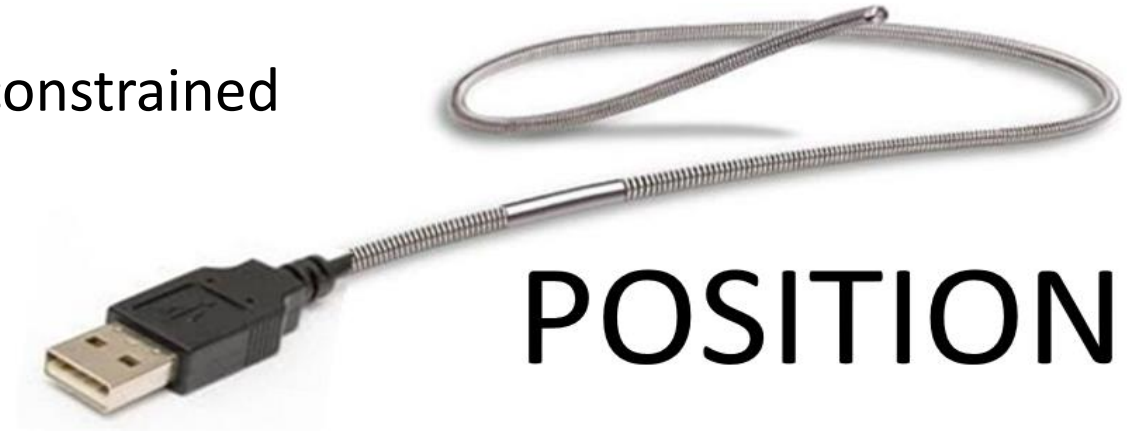


- On-chip behavioral tree to self-configure sensing rate, resolution, and compression strategy
  - Produce requested useful information with minimal energy/data rate
- SAR-based sensor frontend:
  - Dynamic consumption (scales with sensing rate)
  - Nyquist operation, sample-to-sample reconfiguration possible

J. De Roose, et al., "Flexible, Self-Adaptive Sense-and-Compress SoC for Sub-microWatt Always-On Sensory Recording," IEEE SSCL, Vol. 3, 2020.

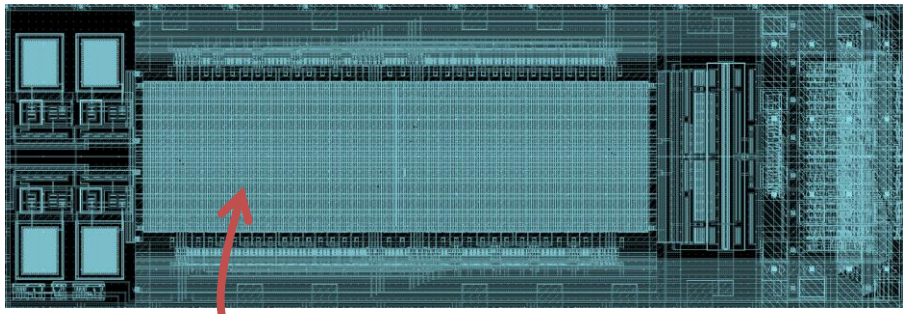
Digital ultrasound catheters

- Power & area constrained
- Array of ADCs

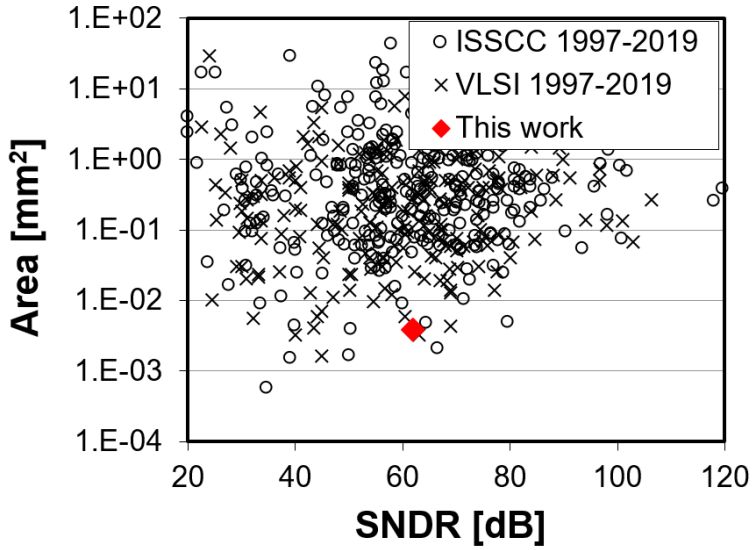


POSITION II

12b 40MS/s ADC in 40nm CMOS: 36 x 108 µm
10b ENOB, 73dB SFDR, 5fJ/conv.step



Delta-length capacitors



Position-II: http://position-2.eu/

Outline

- Introduction, trends & applications
- Low-speed vs high-speed SAR ADCs
- Techniques for power-efficient SAR ADCs
- Application examples
- Limitations and future trends
- Conclusion

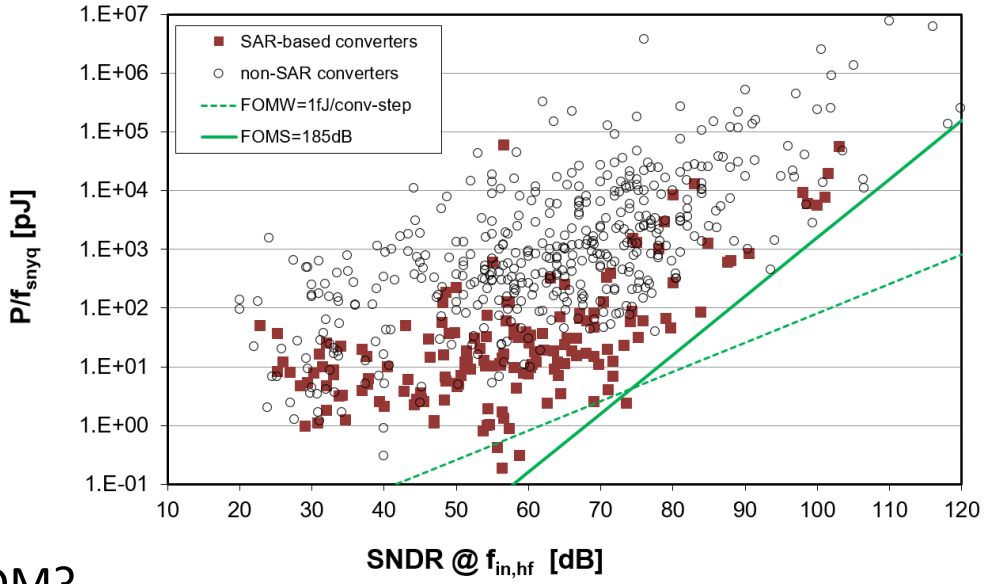
Limitations vs resolution

- SAR can reach high-resolution, but not (yet) best-overall

- Nyquist SAR ADCs
  - Area/Costs high for >16b
  - kT/C cancellation?
  - Calibration

- Noise-shaping SAR ADCs
  - Suitable, relatively new, still lots of progress
  - More aggressive filtering
  - Mismatch-error shaping
  - But is it still a SAR ADC or an SDM?

B. Murmann, "ADC Performance Survey 1997-2020," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.



- Expectation: fading between NS-SAR and SDM implementations

Limitations vs speed

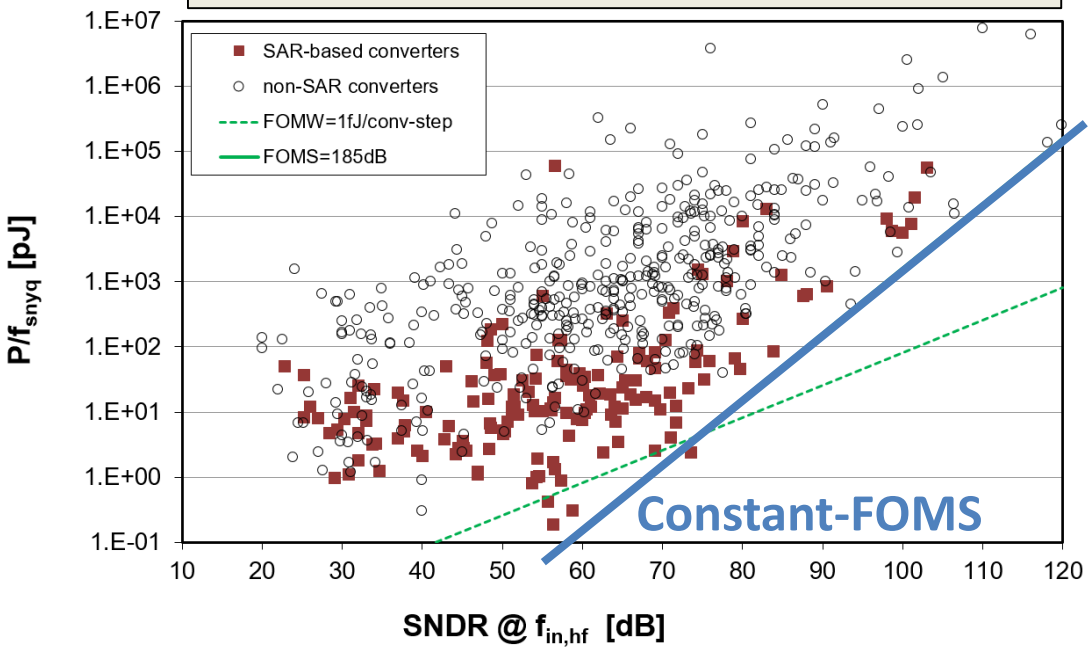
- Time-interleaved SAR ADCs ≈100GS/s
  - Technology scaling still helps
  - Progress over the years is relatively slow
  - Jitter bottleneck

- Expectation: optical/electrical integration

Limitations vs efficiency

- SAR ADC is close to constant-FOMS line
  - Note: not a limit, just a trend
- Potential at low-res (<50dB SNDR)
  - Technology scaling
  - Simplify circuitry
  - Analog circuits
- Potential at high-res (>80dB SNDR)
  - Noise-shaping SAR

B. Murmann, "ADC Performance Survey 1997-2020," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.



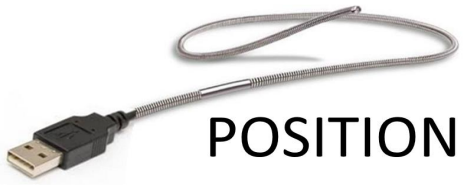
- Expectation: SAR-based ADCs remain leading in efficiency

Conclusion

- SAR ADCs
  - Simple basics
  - Still plenty of ideas and innovation
- Current research: mostly SAR-based ADCs
  - Covers extremely large application space
  - But: basic SAR still attractive for simplicity and efficiency at modest specs
- Future: more blending of architectures, signal types, system integration

Acknowledgements

- Parts of the presented work are funded by:
  - Netherlands Organisation for Scientific Research (NWO), project #16594
  - Phoenix project – EU Horizon 2020 research and innovation programme, grant agreement #665347
  - POSITION-II project



ECSEL Joint Undertaking

Grant no.: Ecsel-783132-Position-II-2017-IA