Dielectric Characterization of Structural and Passivation Films for Flexible CMUT Microfabrication

Ivano Lucarini
Department of Engineering
Roma Tre University
Institute for Microelectronics and Microsystems
CNR
Rome, Italy
ivano.lucarini@uniroma3.it

Francesco Maita
Institute for Microelectronics and Microsystems
CNR
Rome, Italy
luca.maiolo@cnr.it

Luca Maiolo
Institute for Microelectronics and Microsystems
CNR
Rome, Italy
luca.maiolo@cnr.it

Alessandro S. Savoia
Department of Engineering
Roma Tre University
Rome, Italy
alessandro.savoia@uniroma3.it

***Abstract*— Polymer-based CMUT microfabrication approaches allow low-cost fabrication of flexible transducers. However, they are characterized by processing limitations mainly related to the low glass transition temperature of polymers, reducing the possible choice of materials that can be used for electrodes and in-cavity passivation layers, the latter having a major impact on transducer performance and reliability. In this paper, we experimentally evaluate the electrical properties of these two materials in terms of dielectric dispersion and losses, and high electric field response with respect to state-of-the-art materials.**

***Keywords*— CMUT, Flexible, Ambient Temperature Silicon Oxide, Polyimide**

I. INTRODUCTION

Capacitive micromachined ultrasonic transducer (CMUT) technology has enjoyed rapid development in the last decade. Advancements both in fabrication and integration, coupled with improved modelling, has enabled CMUTs to make their way into mainstream ultrasound imaging. Compared to conventional technology, CMUT ultrasound transducers convey numerous advantages such as large bandwidth and efficiency [1], [2], easy fabrication of large arrays and lower cost. The CMUT is a high electric field device, and by controlling the high electric field from issues like charging and breakdown it is possible to have an ultrasound transducer with superior bandwidth and sensitivity, amenable for integration with electronics and manufactured using traditional integrated circuits fabrication technologies with all its advantages. A CMUT device can be made flexible for wrapping around a cylinder or even over human tissue, for example, and all this is possible thanks to the use of polymeric materials such as SU-8 [3], [4], [8] or Polyimide [5], [8]. In this paper, we present the electrical characterization of two dielectric materials of fundamental importance to manufacture a device with the characteristics just mentioned: a silicon oxide (SiO_2) with an excellent response to high electrical fields in terms of charge injection and breakdown, and a thin and flexible polymer with optimal structural and electrical characteristics for the fabrication CMUT devices, i.e. the Polyimide (PI).

II. MICROFABRICATION TECNOLOGY

A. *Microfabrication SU-8 based Process*

In recent years, we have developed a microfabrication process based on SU-8 (SU-8 3003) [8] whose main steps are shown in Fig. 1 and consists in photolithography processes with lift-off and wet etching, which contribute to minimize the costs and the fabrication effort. The CMUT microfabrication is carried out on a silicon wafer, on top of which a flexible substrate, consisting of a 5µm-thick layer of PI (PI2611), is previously spun. The PI, once deposited on a wafer, can be mechanically peeled off from the support together with the structures on it, thus obtaining fully flexible devices.

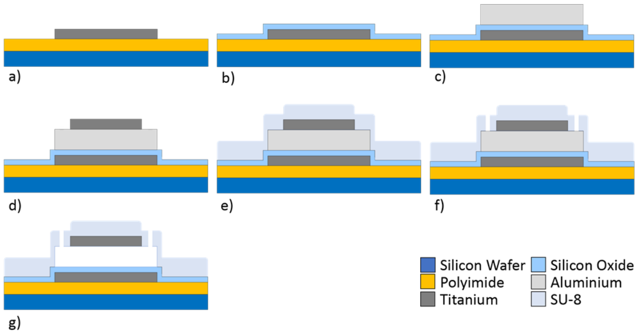

Fig. 1. Fabrication scheme for SU-8 based process: a) Bottom electrode evaporation; b) SiO_2 deposition; c) Aluminium sacrifial layer evaporation; d) Top electrode evaporation; e) SU-8 deposition; f) SU-8 development (etc-holes opening for alluminium removing); g) Alluminium etching.

B. *SU-8 based process limitations*

On SU-8 based CMUT devices we carried out Laser Doppler Vibrometer (LDV) basic electromechanical characterization in air-coupled conditions, which have proven full functionality of all the membranes [8]. This result confirms the possibility to fabricate polymer-based CMUTs using SU-8. Even though the proposed fabrication process was demonstrated to be solid and

---

This work is part of the POSITION-II project funded by the ECSEL Joint Undertaking under grant number Ecsel-783132-Position-II-2017-IA.

978-1-7281-5448-0/20/$31.00 ©2020 IEEE

reproducible, the etch holes used to remove the copper sacrificial layer were still open at the end of the manufacturing process, causing air damping and stiffening effects, which made the behaviour of these devices difficult to predict.

C. Revised Process

We have addressed the above issue by establishing an improved version of the process, in which the SU-8 has been replaced by Polyimide, in order to be able to close the etch-holes at the end of the process.

A high-quality SiO_2 thin layer, deposited at room temperature by Electron Cyclotron Resonance Plasma-Enhanced Chemical Vapor Deposition (ECR-PECVD), is used for in-cavity passivation in the event of contact between the electrodes.

As already demonstrated previously [7], this oxide has an excellent response to high intensity electric fields. Over the last few years, the growth process of this oxide has been fine-tuned in order to create an even more resistant oxide despite the low temperature at which the entire process takes place. In fact, this oxide has grown at room temperature and the highest temperatures reached during the process are of the order of 100-150 °C and are due to the heat of the plasma used to deposit material on the substrate.

The need to have a vacuum cavity device has shifted the choice of polymer from SU-8 to PI. Thanks to the PI it will be possible to close the holes for the removal of the sacrificial metal and have a vacuum cavity not affected by air damping and stiffening effects.

III. DIELECTRIC CHARACTERIZATION

In the process actually under development, the in-cavity bottom electrode passivation is achieved by a thin SiO_2 layer grown by ECR-PECVD at room temperature. The top electrode is supported by a thin layer of PI, which also has the function of electrically isolating it from the bottom electrode across the entire device. To evaluate the electrical properties of the two dielectric materials, we fabricated and characterized test capacitors (Fig. 2) where dielectric material is sandwiched between a 150nm-thick Titanium layer and a series of 1µm-thick, 500µm-diameter copper dots. The SiO_2 and the PI are respectively 100nm- and 2µm-thick. In order to quantitatively evaluate dielectric dispersion and losses, we carried out impedance measurements on both test capacitors as a function of frequency using a 100mV amplitude signal. These measurements were acquired at different bias voltages in the 0-20V range, using a HP4192A (Hewlett-Packard Inc., Palo Alto, CA, USA). Plots of Fig. 3 have been obtained from these measurements and show the value of the dielectric dissipation factor (DF) as a function of the frequency at different bias voltage values.

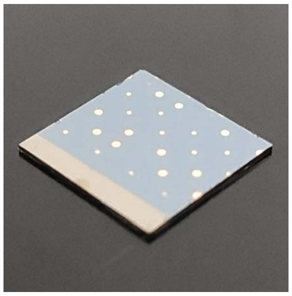

Fig. 2. Test Capacitor: dielectric material is sandwiched between 150 nm tick Titanium film and half millimiter diameter copper dots.

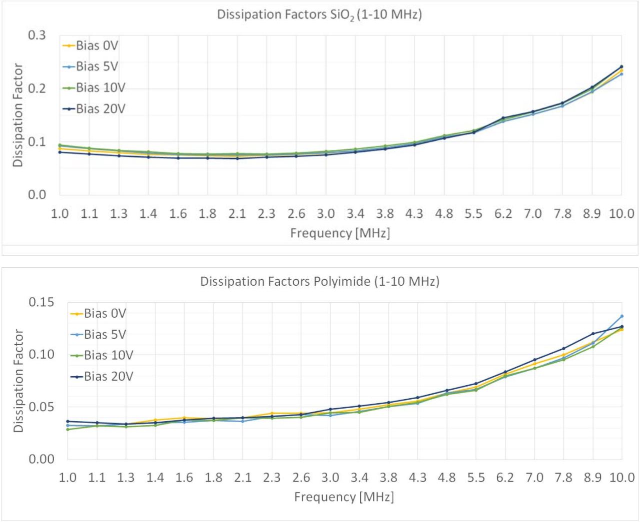

Fig. 3. Dissipation factor for SiO_2 and PI. These values were obtained from capacitance measurements as a function of the oscillation frequency of a signal with an amplitude of 100 mV, at different DC bias values, in the range 1-10 MHz.

On the SiO_2 capacitor, we performed electrical tests by applying an increasing voltage up to 100 V across the electrodes using a ramp rate of 0.1 V/s, and by measuring the leakage current. The current as a function of the electric field (Fig. 4) was computed from the measured I/V characteristic, acquired using a HP4140B (Hewlett-Packard Inc., Palo Alto, CA, USA).

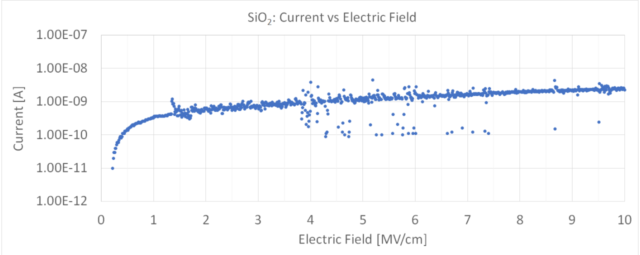

Fig. 4. Leakage current as a function of electric field. In the range 0 - 1 MV/cm we have the majority of the charge injection. In the range 1-10 MV/cm the dielectric shows an excellent response to the electric field without highlighting other important charge injections.

IV. RESULTS AND CONCLUSIONS

We estimated the DF for both materials, which shows a growing trend between the values 0.07 and 0.24 for SiO_2, and between 0.03 and 0.13 for PI in the range 1-10 MHz. In both cases, we observe how the DF increases together with the frequency. The higher the DF in the CMUT in-cavity passivation materials, the higher the resistive shunt impedance, which causes loss of efficiency in the device operation. In the specific case of the two dielectrics under examination, loss effect becomes higher as the frequency increases. On the other hand, DF is practically constant as the bias voltage varies. We are currently evaluating quantitatively the effects of the estimated DF on realistic CMUT configurations.

In SiO_2 we observed most of the charge injection for electric fields in the range 0 - 1 MV/cm. In the range 1-10 MV/cm the dielectric shows an excellent response to the electric field without highlighting other important charge injections and showing leakage currents in the order of nano amperes. All this proves that ECR-PECVD SiO_2 grown at room temperature has a high electric field resistance, resulting in better performance as compared to thermal SiO_2 or to state-of-the-art Dual-Frequency PECVD Silicon Nitride [6], which presents a second important charge injection starting from 2.5 MV/cm [7]. We believe that ECR-PECVD will enable the fabrication of highly reliable flexible CMUTs for medical applications up to the MHz range.

REFERENCES

[1] M.I. Haller, B.T. Khuri-Yakub, “A surface micromachined electrostatic ultrasonic air transducer,” in *Proc. IEEE Ultrason Symp.*, 1994, pp. 1241–1244.

[2] A. Caronti, G. Caliano, R. Carotenuto, A. Savoia, M. Pappalardo, E. Cianci, and V. Foglietti., “Capacitive micromachined ultrasonic transducer (CMUT) arrays for medical imaging,” *Microelectronics Journal* 37, 2006, pp. 770–777.

[3] C. Ge, E. Cretu, “Design and fabrication of SU-8 CMUT arrays through grayscale lithography,” *Sens. Actuators, A*, vol. 280, no. 2, 2018, pp. 368-375.

[4] C. D. Gerardo, E. Cretu, R. Rohling, “Fabrication and testing of polymer-based capacitive micromachined ultrasound transducers for medical imaging,” *Microsystems & Nanoengineering*, vol. 4, no. 1, 2018. p. 19.

[5] A. Pecora, L. Maiolo, M. Cuscunà, D. Simeone, A. Minotti, L. Mariucci, G. Fortunato, “Low-temperature polysilicon thin film transistors on polyimide substrates for electronics on plastic,” *Solid State Electron.*, 2008, pp. 348–352.

[6] A. Savoia, G. Caliano, R. Carotenuto, C. Longo, P. Gatta, A. Caronti, E. Cianci, V. Foglietti, and M. Pappalardo, "Enhanced echographic images obtained improving the membrane structural layer of the cMUT probe," in *Proc. IEEE Ultrason. Symp.*, 2005, vol. 4, pp. 1960-1963.

[7] A. S. Savoia, B. Mauti, G. Caliano, L. Maiolo, A. Minotti, A. Pecora, G. Fortunato, A. Bagolini, P. Bellutti, “Optimization of the Efficiency and Reliability of Reverse-Fabricated CMUT Arrays”, in *Proc. IEEE Ultrason. Symp.*, 2017.

[8] I. Lucarini, L. Maiolo, A. S. Savoia, “Fabrication and Characterization of Capacitive Micromachined Ultrasonic Transducers Integrated on Ultra-thin and Flexible Substrates”, in *Proc. IEEE Ultrason. Symp.*, 2019.